1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,MACBOOK PRO 17"

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

9/26/2006

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36 38	PATA Connector	(MASTER) (MASTER)
37 39	FireWire Link (TSB83AA22)	M59_MLB 09/15/2006
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64 78	1.8V Supply	(MASTER) (MASTER)
65 79	3.3V / 1.05V Power Supplies	(MASTER) (MASTER)
66 80	3.3V G3Hot Supply & Power Control	M59_MLB 09/15/2006
67 81	Power Aliases	(MASTER) (MASTER)
68 82	DC-In & Battery Connectors	(MASTER) (MASTER)
69 83	PBus Supply & Batt. Charger	M59_LIO 09/15/2006
70 84	ATI M56 PCI-E	(MASTER) (MASTER)
71 85	GPU (M56) Core Supplies	(MASTER) (MASTER)
72 86	ATI M56 Core Power	(MASTER) (MASTER)
73 87	ATI M56 Frame Buffer I/F	(MASTER) (MASTER)
74 88	GPU Straps	M57_MLB_MG 08/08/2006
75 89	GDDR3 Frame Buffer A	(MASTER) (MASTER)
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77 91	ATI M56 GPIO/DVO/Misc	(MASTER) (MASTER)
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ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7164	1	SCHEM,TRUCKEE,M57	SCH	CRITICAL	
820-2059	1	PCBF,TRUCKEE,M57	PCB	CRITICAL	

DRAWING
TITLE=TRUCKEE
ABBREV=DRAWING
LAST_MODIFIED=Tue Sep 26 13:17:56 2006

DIMENSIONS ARE IN MILLIMETERS
XX ± ____
X.XX ± ____
X.XXX ± ____
ANGLES ± ____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEMATIC,MACBOOK PRO 17

DRAWING NUMBER 051-7164 REV. 06004

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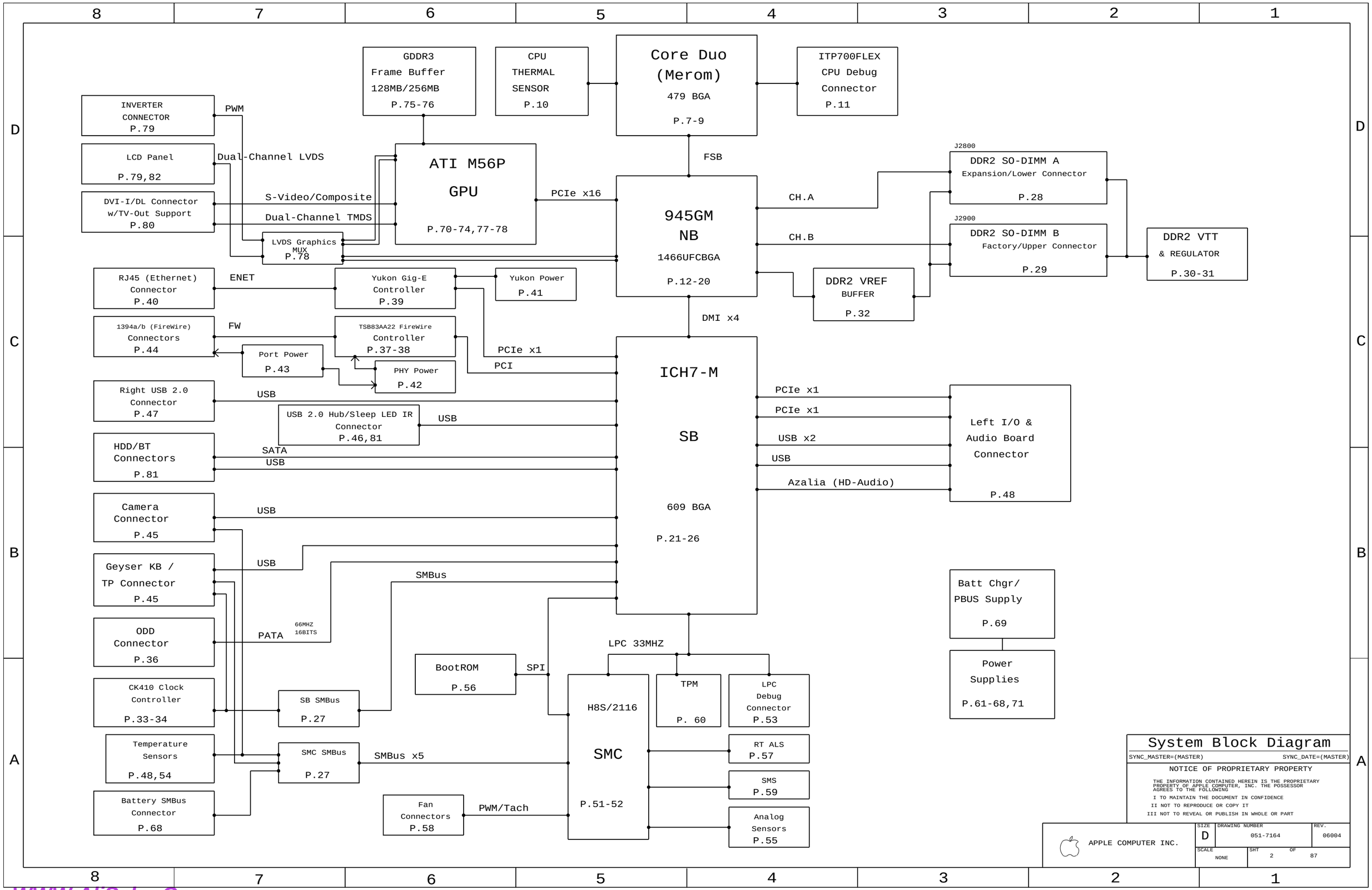

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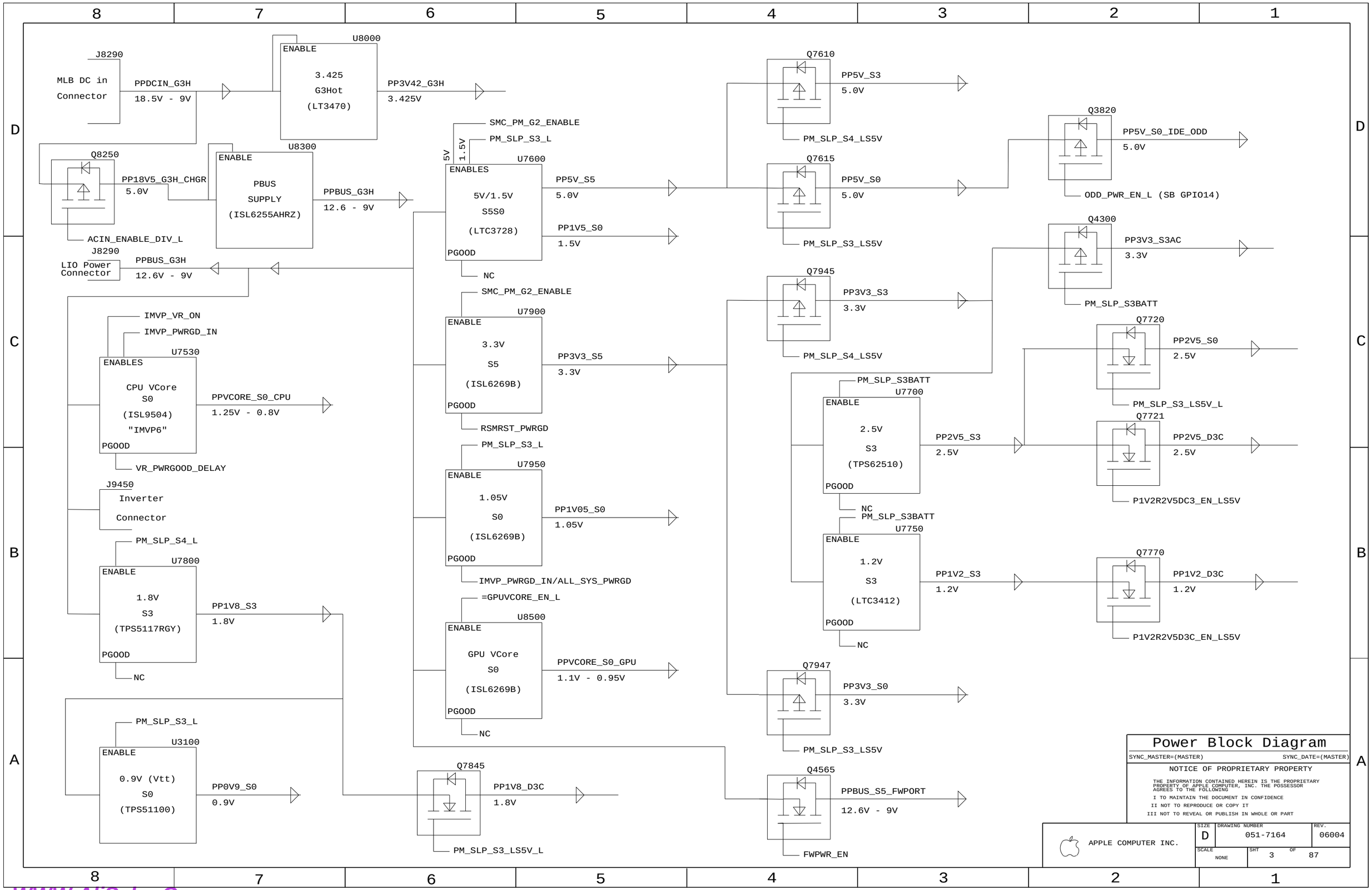

Power Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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BOM NUMBER	BOM NAME	BOM OPTIONS
630-7814	TRUCKEE,2.33GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJK

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG

BOM GROUP	BOM OPTIONS
M57_COMMON	ALTERNATE,COMMON,M57_COMMON1,M57_COMMON2,M57_COMMON3,M57_COMMON4,M57_DEBUG
M57_COMMON1	ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL,D3CPGOOD_3V3,ISL6255A,NO_3G
M57_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M57_COMMON3	LVDS_PD,FW_PORT_FAULT_PU
M57_COMMON4	BOOTROM_DEVEL,SMC_PRGRM
M57_DEBUG	ITP,LPCPLUS
M57_TPM	TPM

BAR CODE LABELS / EEE #'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WJK]	CRITICAL	EEE_WJK

MODULE PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0368	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON

ALTERNATE PARTS

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445		ALL	SI7806ADN for FDM6296
128S0083	128S0073		C2516	1.86 MAX ALT TO 1.9 MAX
128S0093	128S0092		ALL	KEMET IS ALT TO SANYO
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504
152S0287	152S0435		ALL	Alternates for Coilcraft MSS5131

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1931	1	IC,PRGRM,SMC(NEW),M57	U5800	CRITICAL	SMC_PRGRM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED ,M57	U6301	CRITICAL	BOOTROM_DEVEL
341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL
353S1461	1	IC,ISL9504,SYNC REG CTL,QFN 48	U7530	CRITICAL	
359S0109	1	IC,LOW POWER CLOCK SYNTHESIZER,68PIN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3393	1	IC,MDC,B2,PRQ,2.33GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	

Extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

BOM CONFIGURATION

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	61C7
TRUE		P5VS5_RUNSS	62C5 66A6
TRUE		P1V5S0_RUNSS	62C4 66C6
TRUE		P2V5S3_MODE	
TRUE		P2V5S3_SHDNRT	
TRUE		P1V2S3_RT	63B6
TRUE		P1V2S3_RUNSS	41C4 63B7
TRUE		P1V8S3_COMP	
TRUE		P1V8S3_FSET	
TRUE		P3V3S5_COMP	65C6
TRUE		P3V3S5_FSET	65D6
TRUE		P1V05S0_COMP	65A7
TRUE		P1V05S0_FSET	65B7
TRUE		P3V42G3H_FB	66C3
TRUE		GPUVCORE_COMP	71C7
TRUE		GPUVCORE_FSET	71C7
TRUE		GPUBBP_ADJ	71B7

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 87D6
TRUE		FSB_ADS_L	7D6 12C4 87D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 87C6
TRUE		FSB_BNR_L	7D6 12C4 87D6
TRUE		FSB_BREQ0_L	7D6 12C4 87D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 87D6
TRUE		FSB_DBSY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_DRDY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_HIT_L	7D6 12B4 87D6
TRUE		FSB_HITM_L	7D6 12B4 87D6
TRUE		FSB_LOCK_L	7D6 12B4 87D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 87D6

EXPOSED_VIA property indicates that the net
should have a via with 10-mil soldermask
opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 33B4 34C3 34C5
TRUE	SB_CLK100M_SATA_N	21B6 33B4 34C3 34C5
TRUE	USB_BT_P	6C1 6C2 6C3 22C2 81A4
TRUE	USB_BT_N	6C1 6C2 6C3 22C2 81A4

Misc NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		USB2_CAMERA_P_F	45B5
TRUE		USB2_CAMERA_N_F	45B5
TRUE		TP_FW_CTL<0>	37C3

Functional Test Points

Power Nets

FUNC_TEST		
TRUE	PP0V9_S0	19D3 34B8 34C3 34C8 35B4 65A2 67D6 67D8
TRUE	PP1V05_S0	19D3 19D6 19D8 19D9 19E3 19E5 19E6 19E7 19E8 19E9 19F4 19F5 19F6 19F7 19F8 19F9 19G4 19G5 19G6 19G7 19G8 19G9 19H4 19H5 19H6 19H7 19H8 19H9 19J4 19J5 19J6 19J7 19J8 19J9 19K4 19K5 19K6 19K7 19K8 19K9 19L4 19L5 19L6 19L7 19L8 19L9 19M4 19M5 19M6 19M7 19M8 19M9 19N4 19N5 19N6 19N7 19N8 19N9 19P4 19P5 19P6 19P7 19P8 19P9 19R4 19R5 19R6 19R7 19R8 19R9 19T4 19T5 19T6 19T7 19T8 19T9
TRUE	PP1V2_D3C	11B3 11C5 12A7 12B7 12C2 19C8 19D1 19D2 19D5 19D6
TRUE	PP1V2_S3	5A4 39A8 39D7 63B3 67D6 67D8
TRUE	PP1V5_S0	19C5 19D3 19D2 19D5 19D6 19D7 19D8 19D9 19E4 19E5 19E6 19E7 19E8 19E9 19F4 19F5 19F6 19F7 19F8 19F9 19G4 19G5 19G6 19G7 19G8 19G9 19H4 19H5 19H6 19H7 19H8 19H9 19J4 19J5 19J6 19J7 19J8 19J9 19K4 19K5 19K6 19K7 19K8 19K9 19L4 19L5 19L6 19L7 19L8 19L9 19M4 19M5 19M6 19M7 19M8 19M9 19N4 19N5 19N6 19N7 19N8 19N9 19P4 19P5 19P6 19P7 19P8 19P9 19R4 19R5 19R6 19R7 19R8 19R9 19T4 19T5 19T6 19T7 19T8 19T9
TRUE	PP1V5_S0_NB	
TRUE	PP1V8_S3	31C5 32C6 37B2 64A6 64C1
TRUE	PP1V8_D3C	29B2 34C2 35B6 39D2 39D3 39D4 39D5 39D6 39D7 39D8 67B6 67B8 64A4 67B6 67B8 72B8 73A5 73A8 73B5 73B8 75D5 75D6 76D5 76D8 82D7
HZ0)	PP2V5_S0	17C6 17D6 19A4 19A6 19A8 19C5 19D7 63D1 66B6 67A6 67A8 67B6 82C5 82D3
TRUE	PP2V5_D3C	63C1 67A6 67A8 77A8 77C6 78C8 82D7
TRUE	PP3V3_S0	
TRUE	PP3V3_S3	
TRUE	PP3V3_S5	65D8 66C5 67C3 67D3 67D5 79D5 24C3 25B6 25C8 25D2 25D3 25E5 11B6 22C6 22D8 23A7 23B7 23D1 23B4 23D8 24A5 24B3 24B5 24C4 24D3 24E4 63D4 63D8 65C8 65D1 65D2
TRUE	PP5V_S0	
TRUE	PP5V_S3	5B2 45C3 52B8 62A2 67B1 67B3 81C4 81C6
TRUE	PP5V_S5	60B8 60D6 67B1 67C1 67C3 69C8 47D7 62B5 62A1 62B2 62B6 62C8 64C8 65B7 65D6 71D7
TRUE	PPBUS_G3H	6A1 41C6 42B8 43D8 59D3 61D4 61D7 62D7 64A6 64D7 65B7 65D6 67C5 68D5 69C1 71D7 79B7
TRUE	GND	

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TRUE	IMVP_VR_ON	51D7 61C7
TRUE	IMVP_DPRSLPVR	61C7 87C6
TRUE	PM_SLP_S3_L	66C8 27C3 32B3 39C8 42A8 43C8 51C5 59C3 65B8 66B6 66C7
TRUE	PM_SLP_S3BATT	41B5
TRUE	PM_SLP_S4_L	66B8 66C1 6A1 6A2 23C3 41B6 47C7 48C3 51C5 64C8 66A6
TRUE	PM_SLP_S5_L	23C3 51C5 52A2
TRUE	P1V5P1V05S0_PGOOD	61C7 65B8 66B2 66B3 66B5
TRUE	CPU_DPRSTP_L	7B3 21C4 61C7
TRUE	IMVP6_VID<6..0>	9C1 61C7
TRUE	FSB_CLK_CPU_N	7C6 33C4 34D3 34D5
TRUE	FSB_CLK_CPU_P	7C6 33C4 34D3 34D5
TRUE	PLT_RST_L	82A4 2CA4 6C6 6C7 14B7 22A6 26A4 26B1 26C1 26C3 79A8
TRUE	PLT_RST_L	5C4 6C6 6C7 14B7 22A6 26A4 26B1 26C1 26C3 79A8
TRUE	PEG_RESET_L	26B1 70A5 82A4
TRUE	SMC_LRESET_L	26B1 51C7
TRUE	TPM_LRESET_L	26B1 60B7
TRUE	CPU_STPCLK_L	7C8 21C4 87C6
TRUE	FSB_CLK_NB_P	12A6 33C4 34D3 34D5
TRUE	FSB_CLK_NB_N	12A6 33C4 34D3 34D5
TRUE	CLK_NB_OE_L	14B6 33B4
TRUE	NB_CLK100M_GCLKIN_P	14C4 33B4 34C4 34C5
TRUE	NB_CLK100M_GCLKIN_N	14C4 33B4 34C4 34C5
TRUE	NB_CLK_DREFCLKIN_P	14C4 34B2 34B4
TRUE	NB_CLK_DREFCLKIN_N	14C4 34B2 34B4
TRUE	NB_CLK_DREFSSCLKIN_P	14B4 33B4 34B4 34B5
TRUE	NB_CLK_DREFSSCLKIN_N	14C4 33B4 34B4 34B5
TRUE	CPU_THERMTRIP_R	21C2
TRUE	TP_SB_SUS_CLK	6C6 6C7 23C3

MAC-1 TPs

FUNC_TEST		
TRUE	CPU_PWRGD	7B3 21C4 87C6
TRUE	TP_CPU_CPUSLP_L	21C4
TRUE	PM_DPRSLPVR	14B7 23C3 61C8 87C6
TRUE	CPU_DPSLP_L	7B3 21C4 87C6
TRUE	PM_LAN_ENABLE	23C3 51D7
TRUE	PCI_RST_L	22A6 37C2
TRUE	PM_RSMRST_L	23C1 51D7
TRUE	PM_SB_PWROK	23C3 26A6
TRUE	SB_RTC_RST_L	21D6 26D4
TRUE	PM_STPCPU_L	23C8 33C4
TRUE	PM_STPPCI_L	23C8 33C4
TRUE	VR_PWRGD_CK410	23C5 26B8
TRUE	VR_PWRGOOD_DELAY	14B6 26B5 61C7
TRUE	FSB_CPURST_L	7D6 11B5 12C4 87D6
TRUE	FSB_SLPCPU_L	7A3 12A4
TRUE	FSB_DPWR_L	7B3 12B4 87D6
TRUE	NB_SB_SYNC_L	14B6 22A6
TRUE	PP2V5_S0_GPU_TPVDD	78C7
TRUE	PP2V5_S0_GPU_TXVDDR	78C7
TRUE	PP2V5_S0_GPU_AVDD	78C7
TRUE	PP2V5_S0_GPU_A2VDD	78B7
TRUE	PP2V5_S0_GPU_LPVDD	78B7 66B6 67A3 67B3 67C3 67C5 71D2 79A8 79D3
TRUE	PP2V5_S0_GPU_LVDDR	78B7 26B4 26B6 26B8 26D1 27C3 27D3 24A3 25A3 25B3 24B3 24B5 24C3 25A4 25B4
TRUE	PP3V3_S0	29A4 29B4 (=PP3V3_S0_CK410)
TRUE	PP3V3_S0_CK410_VDD48	1AC7 1AD6 1YC6 1YC7 1YD6 1YD7 21C3 21D3 22B5 23B3 23D5 27B8 27C4 27D2 27D4 27D8 49B4 49C4 49C7 52D3 54B5 49B5 49C4 49C7 52D3 54B5 62A6 65B1 65D6 66B1 66B5 82A4 82B3 82C6 82D5
TRUE	PP3V3_S0_CK410_VDD_PCI	33C5
TRUE	PP3V3_S0_CK410_VDD_REF	
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC	
TRUE	PP3V3_S0_CK410_VDDA	
TRUE	PP3V3_FWPHY	6C3 6C5 6C6 38B5 38D7 42C4 43B8 44A8 44B8
TRUE	PP3V3_FWPHY_AVDD	38D5
TRUE	PP3V3_FWPHY_PLLVDD	38C6
TRUE	PP1V95_FWPHY	6C3 6C5 6C6 38B2 38D5 42C1
TRUE	PP1V95_FWPHY_PLLVDD	38D3
TRUE	PP1V2_S3	5D4 39A8 (=PP1V2_S3_ENET) 39D7 63B3 67D6 67D8
TRUE	PP3V3_S3AC	39A5 39B4 (=PP3V3_S3_ENET) 39B5 39B8 39D6 39D8 42C4 67D1 67D3
TRUE	PP2V5_S3	39D3 63C3 (=PP2V5_S3_ENET) 63D3 63D4 67B6 67B8
TRUE	PP2V5_S3_ENET_AVDD	39D5 40D5

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	71A4 78B8 80A1 80B5 81B7 5D3 5D4 25D8 31D1 62D1 62D5 64 25D8 31C5 36D5 53C4 55A8 57B5 60B5 67A1 67B1 67B3
TRUE	FAN_LT_PWM	19D7 21C1 24C3 24D3 25C4 58B6
TRUE	FAN_LT_TACH	58B6
TRUE	FAN_RT_PWM	19D7 62A7 67B6 67C6 67C8 58B3
TRUE	FAN_RT_TACH	58B3

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	66D2 67D3 67D5 68B8 69A8 69B8 69C8 81D4 26D6 27C3 35B7 47B5 51C2 61D3 61D4 62B1 62B5 62B7 67B3 71A6 79B8 80A1 80B5 81B3 52D7 53C4 66A8 66C8 62B2 66A4 25D8 31C5 36D6 53C4 55A8 57B5 60C4 58C7 61D7 62B1 66B5 67A1 67B1
TRUE	PP5V_S0	24B5 25A5 25B2 25D6 25E3 25G2 48B6 67C6 67C8
TRUE	LPC_AD<0>	21D4 51D7 53C4 60C6
TRUE	LPC_AD<1>	21D4 51D7 53C4 60C6
TRUE	LPC_FRAME_L	21C5 51C7 53C4 60C6
TRUE	PM_CLKRUN_L	23C8 51C5 53C4 60C6
TRUE	BOOT_LPC_SPI_L	22B3 51C7 53B4
TRUE	SMC_TMS	51B5 52B2 53B4
TRUE	DEBUG_RST_L	26B1 53B4
TRUE	SMC_TRST_L	51C1 53B4
TRUE	SMC_TDO	51B5 52B2 53B4
TRUE	SMC_MD1	51C1 53B4
TRUE	SMC_TX_L	47B5 51C7 52B2 52B3 53B4
TRUE	FWH_INIT_L	21C4 51D5 52D3 52D5
TRUE	PCI_CLK_PORT80_LPC	34D6 53C5
TRUE	LPC_AD<2>	21D4 51C7 53C5 60C6
TRUE	LPC_AD<3>	21D4 51C7 53C5 60C6
TRUE	INT_SERIRQ	23C8 51C7 53C5 60C6
TRUE	PM_SUS_STAT_L	23C5 51C5 52A2 53B5 60C6
TRUE	SMC_TDI	51B5 52B2 53B5
TRUE	SMC_TCK	51C5 52B2 53B5
TRUE	SMC_RST_L	51C3 52D6 53B5
TRUE	SMC_NMI	51C1 53B5
TRUE	SMC_RX_L	47B5 51C7 52B2 52B3 53B5
TRUE	SV_SET_UP	23B6 23C3 53B5

Resistor Calibration

FUNC_TEST		
TRUE	PP5V_S0_ISENSECAL	67D8 25C4 55A4 65A2 67D6 25C4 25D3 34B8 34C6 19D7 21C1 24C3 24D3 25C4 19D7 62A7 67B6 67C6 67C8
TRUE	PP1V8_S3	19D7 21C1 24C3 24D3 25C4
TRUE	PP1V05_S0	19D7 62A7 67B6 67C6 67C8
TRUE	PPVCORE_S0_CPU	8B5 8D7 9D7 55A6
TRUE	PPVCORE_D3C_GPU	55D7 61D1 67D1 67D3
TRUE	ISENSE_CAL_EN	55A5 55C7 67A6 67A8 71B7 71C1 72D8 77A7
TRUE	GND	51B7 55A8

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TRUE	PP5V_S3	5D4 45C8 52B8 62A2 67B1 67B3 81C4 81C6
TRUE	USB2_CAMERA_N	6D1 6D2 6D3 22C2 45C3
TRUE	USB2_CAMERA_P	6D1 6D2 6D3 22C2 45B3
TRUE	PP5V_S3_CAMERA_F	45C5

Inverter Connector

TRUE	GND_CHASSIS_INVERTER	5B2 6A6 6A8 45B5 45C5 79A5 79A6
TRUE	PPBUS_S0_INVERTER	79B5
TRUE	PP5V_INVERTER_SW	79B5
TRUE	INVERTER_PWM	79A5
TRUE	GND_CHASSIS_INVERTER	5B2 6A6 6A8 45B5 45C5 79A5 79A6

Thermal Sensors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	54C5
TRUE	HSTHMSNS_DX_N	54C5
TRUE	RSFSTHMSNS_D_P	54D5
TRUE	RSFSTHMSNS_D_N	54C5

SMC TPs

FUNC_TEST		
TRUE	PM_SYSRST_L	23C5 26C5 51B7
TRUE	SMC_ONOFF_L	51C5 52B2 52C6 81C4

Battery Connector

FUNC_TEST		
TRUE	BATT_POS	68A1 68A2 69B1
TRUE	BATT_NEG	68B1 68B2
TRUE	SMC_BS_ALRT_L	51C5 52B2 68B2
TRUE	SMBUS_SMC_BSA_SCL	27C1 27C2 27C3 51B5 68B2
TRUE	SMBUS_SMC_BSA_SDA	27C1 27C2 27C3 51B5 68B2

Left I/O Data Connector

FUNC_TEST		
TRUE	PP1V5_S0	62A8 62C1 66C5 66D6 66E3 66G6 24A3 24A5 24B5 25A5 25B2 25D6 25E3 25G2 48B6 67C6 67C8
TRUE	ALS_GAIN	6D5 48C4 51B5
TRUE	LTALS_OUT	48C3 57C7
TRUE	ACZ_SDATAIN<0>	21C7 48B3 87B4
TRUE	ACZ_SDATAOUT	21C7 48B3 87B4
TRUE	ACZ_BITCLK	21C7 48B3 87B4
TRUE	ACZ_RST_L	21C7 48B3 87B4
TRUE	EXCARD_OC_L	6C1 6C3 22C4 22D8 48C3 52B3
TRUE	LTUSB_OC_L	60I 6G3 22C4 22D8 48C3
TRUE	LT2USB_OC_L	6C1 6C3 22C4 22D8 48C3
TRUE	PM_SLP_S3_LS5V	6A1 6A2 48C3 62B3 66C6 66C7
TRUE	PM_SLP_S4_L	5C4 6A1 6A2 22C3 47C7 48C3 51C5 66A6 66B8
TRUE	SYS_ONEWIRE	48C3 51B7
TRUE	MINI_CLKREQ_L	33B4 34A3 52B2
TRUE	SMC_EXCARD_CP	33A4 48C3 48C3 51B7 52A2
TRUE	EXCARD_CLKREQ_L	33B4 34A3 34A4 48C3
TRUE	SMC_EXCARD_PWR_EN	48C3 51B7
TRUE	LIO_PLT_RESET_L	26C1 48C3
TRUE	ACZ_SYNC	21C7 48B3 87B4
TRUE	USB2_LT_N	6D1 6D2 6D3 22C2 48C6
TRUE	USB2_LT_P	6D1 6D2 6D3 22C2 48C6
TRUE	USB2_EXCARD_N	6C1 6C2 6C3 22C2 48C6
TRUE	USB2_EXCARD_P	6C1 6C2 6C3 22C2 48C6
TRUE	PCIE_EXCARD_R2D_C_N	48B6 50C5 50C6
TRUE	PCIE_EXCARD_R2D_C_P	48B6 50C5 50C6
TRUE	PCIE_EXCARD_D2R_N	22D4 48B6 50B3 50B5 50B6
TRUE	PCIE_EXCARD_D2R_P	22D4 48B6 50C3 50C5 50C6
TRUE	PCIE_CLK100M_EXCARD_P	33B4 34C3 34C5 48B6
TRUE	PCIE_CLK100M_EXCARD_N	33B4 34B3 34B5 48B6
TRUE	USB2_LT2_N	6C1 6C2 6C3 22C2 48C6
TRUE	USB2_LT2_P	6C1 6C2 6C3 22C2 48C6
TRUE	PCIE_MINI_R2D_C_N	48C6 50C5 50C6
TRUE	PCIE_MINI_R2D_C_P	48C6 50C5 50C6
TRUE	PCIE_MINI_D2R_N	22D4 48C6 50C3 50C5 50C6
TRUE	PCIE_MINI_D2R_P	22D4 48C6 50C3 50C5 50C6
TRUE	PCIE_CLK100M_MINI_P	33B4 34D4 34D5 48C6
TRUE	PCIE_CLK100M_MINI_N	33B4 34D4 34D5 48C6
TRUE	SMBUS_SB_SCL	46B6 48B3 81C3
TRUE	SMBUS_SB_SDA	28A6 29A6 33B6 57D6 57D8 57D9 57D6
TRUE	PCIE_WAKE_L	23C8 39C6 48C3
TRUE	SMC_BC_ACOK	48C3 51C5 52A2
TRUE	SMBUS_SMC_A_S3_SCL	27C3 27C5 27C6 48B6 51B5
TRUE	SMBUS_SMC_A_S3_SDA	27B3 27C3 27C5 27C6 48B6 51B5

Left I/O Power Connector

FUNC_TEST		
TRUE	PP18V5_DCIN	68B8 68C5
TRUE	PPBUS_G3H	61D7 62D7 64A6 64C8 65A6 65C7 65D4 64D7 65B7 65D6 69C1 71C7 71D7 79B7
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 5 OF 87

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NC_CPU_A32_L
NC_CPU_A33_L
NC_CPU_A34_L
NC_CPU_A35_L
NC_CPU_A36_L
NC_CPU_A37_L
NC_CPU_A38_L
NC_CPU_A39_L
NC_CPU_APM0_L
NC_CPU_APM1_L
NC_CPU_EXTBREF
NC_CPU_HFPLL
NC_CPU_SPARE0
NC_CPU_SPARE1
NC_CPU_SPARE2
NC_CPU_SPARE4

MAKE_BASE=TRUE
NO_TEST=TRUE

NC_MEM_A_A<15..14>
NC_MEM_B_A<15..14>
MEM_A_A<15..14>
MEM_B_A<15..14>

TP_NB_CFG<4..3>
TP_NB_CFG<6>
TP_NB_CFG<8>
TP_NB_CFG<11..10>
TP_NB_CFG<15..14>
TP_NB_CFG<17>
TP_NB_CFG<13..12>
NB_CFG<4..3>
NB_CFG<6>
NB_CFG<8>
NB_CFG<11..10>
NB_CFG<15..14>
NB_CFG<17>
NB_CFG<13..12>

NOTE: NB_CFG<13..12> require test access

TP_SB_SUS_CLK

Inverter PWM Reset Alias

PLT_RST_L

R0600

ALS_GAIN — RTALS_GAIN — RTALS_GAIN
0, 5%, 1/16W, MF-LF, 402

NC_ENET_CTRL12
NC_ENET_CTRL25

Ethernet Powr Management Support

ENET_LOWPWR_EN

R0690

SB_GPIO30 — ENET_LOWPWR_EN
0, 5%, 1/16W, MF-LF, 402

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

FireWire Aliases

PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF

PP3V3_FWPHY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.20 mm

PP1V95_FWPHY
VOLTAGE=1.95V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

SMC_RSTGATE_L
PCI_AD<19> — =FW_PCI_IDSEL
PCI_GNT3_L
PCI_REQ3_L

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P
USB2_RT_N
RTUSB_OC_L

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P
USB_TRACKPAD_N
UNUSED_USB_B_OC_L

USB Port "C" = Left USB 2.0 Port

USB2_LT_P
USB2_LT_N
LTUSB_OC_L

USB Port "D" = Camera

USB2_CAMERA_P
USB2_CAMERA_N
UNUSED_USB_D_OC_L

USB Port "E" = ExpressCard

USB2_EXCARD_P
USB2_EXCARD_N
EXCARD_OC_L

USB Port "F" = USB 1.1 Hub

USB_HUB_P
USB_HUB_N

USB Port "G" = Bluetooth (M13P)

USB_BT_P
USB_BT_N

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P
USB2_LT2_N
LT2USB_OC_L

TP_USB2_3G_P
TP_USB2_3G_N

LVDS Pull Down Aliases

=LVDS_PD_L_CLK_N — LVDS_L_DATA_P<1>
=LVDS_PD_L_CLK_P — LVDS_L_DATA_N<1>
=LVDS_PD_L_DATA_P<0> — LVDS_L_DATA_P<0>
=LVDS_PD_L_DATA_N<0> — LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2> — LVDS_L_DATA_N<2>
=LVDS_PD_L_DATA_N<2> — LVDS_L_DATA_P<2>

=LVDS_PD_U_CLK_N — LVDS_U_DATA_N<1>
=LVDS_PD_U_CLK_P — LVDS_U_DATA_P<1>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1> — LVDS_U_DATA_N<2>
LVDS_U_CLK_N
LVDS_U_CLK_P

MAKE_BASE=TRUE

Base net is PM_SLP_S3_LS5V

PM_SLP_S4_L

Base net is PM_SLP_S4_L

PM_SLP_S3_LS5V

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Chassis connection to be made at the fan cutout near the right ALS. Not stuffed at Proto.

NO STUFF
SH0601, EMI-SPRING, 0G-502620M
GND_CHASSIS_FANFRAME, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
NO STUFF R0601 0, 5%, 1/10W, MF-LF, 402

Chassis connection to be made at the mounting hole northwest of the DVI connector. Plated hole.

ZT0600, 195R106
GND_CHASSIS_DVI_TOP, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
C0600 0.01UF 10% 50V X7R 402
GND_CHASSIS_DVI_TOP
GND_CHASSIS_DVI_TOP
GND

Chassis connection to be made on FW shell

ZT0603, HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
NO STUFF R0602 0, 5%, 1/10W, MF-LF, 402
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT

ZT0604, HOLE-VIA-P5RP25
GND_CHASSIS_ENET, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_ENET
GND_CHASSIS_ENET
GND_CHASSIS_ENET

Chassis connection to be made at the mounting hole southwest of the USB connector. Plated hole.

ZT0601, 195R106
GND_CHASSIS_USB, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602, HOLE-VIA-P5RP25
GND_CHASSIS_LVDS, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
C0602 0.01UF 10% 50V X7R 402
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS

SH0600, OG-503040, SHLD-SM-LF
GND_CHASSIS_INVERTER, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
LEFT CLUTCH BARREL CABLING

Thermal Module Holes

Add one through via per hole to GND or 2 blind vias per side per hole to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Lower Left GPU TM Hole

Frame holes

ZT0612, HOLE-VIA-P5RP25, GND_CHASSIS_LIOFLEX_HOLE, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C0612 0.01UF 10% 50V X7R 402
C0613 0.01UF 10% 50V X7R 402

ZT0613, HOLE-VIA-P5RP25, GND_CHASSIS_ODD_HOLE, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C0610 0.01UF 10% 50V X7R 402
C0611 0.01UF 10% 50V X7R 402

ZT0611, HOLE-VIA-P5RP25, GND_CHASSIS_BATTCONN_HOLE, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_BATTCONN_HOLE
C0619 0.01UF 10% 50V X7R 402
C0614 0.01UF 10% 50V X7R 402

ZT0610, HOLE-VIA-P5RP25, GND_CHASSIS_LNDACARD_HOLE, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C0615 0.01UF 10% 50V X7R 402
C0616 0.01UF 10% 50V X7R 402

ZT0614, HOLE-VIA-P5RP25, GND_CHASSIS_LEFT_DIMM_HOLE, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C0617 0.01UF 10% 50V X7R 402
C0618 0.01UF 10% 50V X7R 402

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 6 OF 87	

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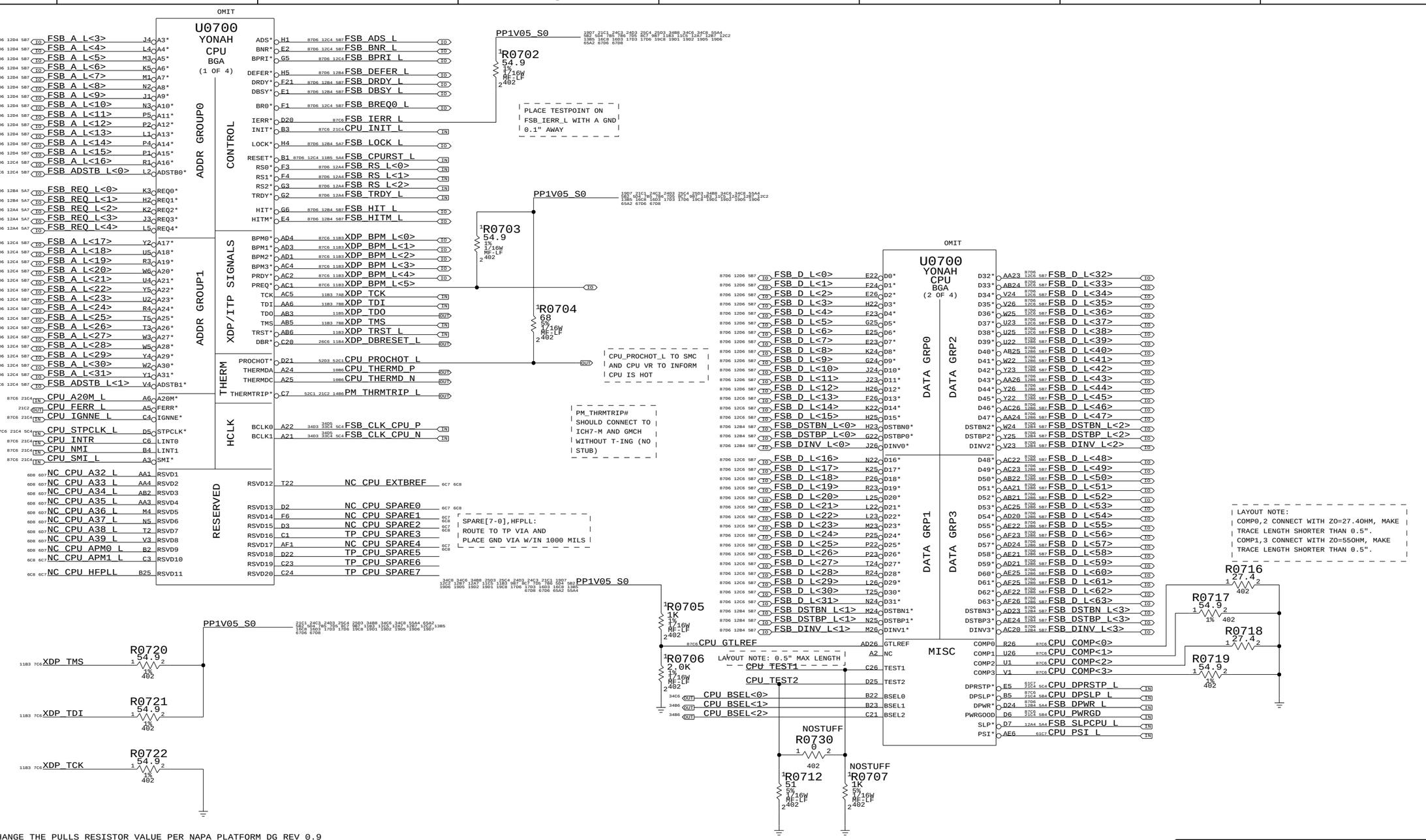

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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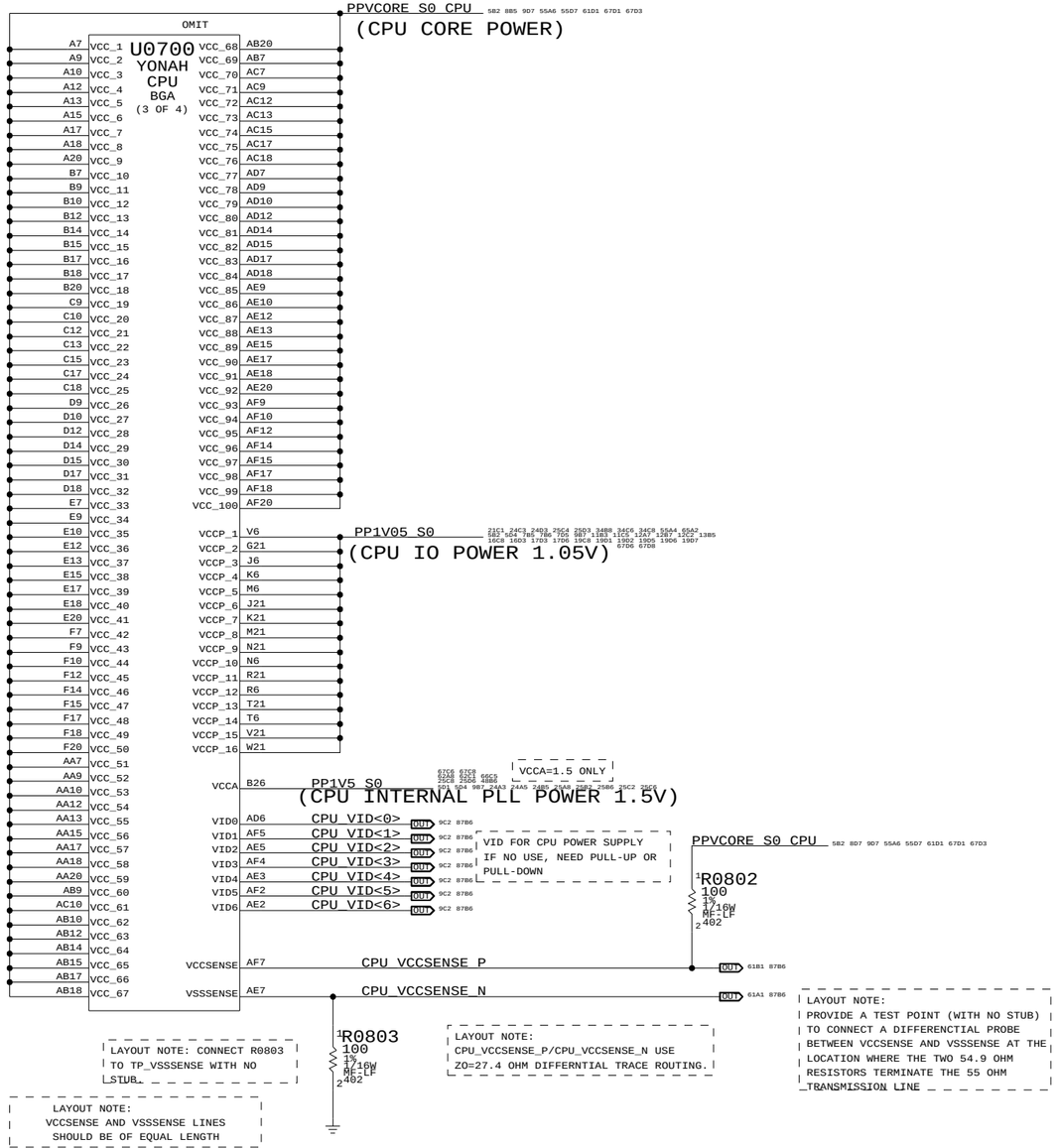

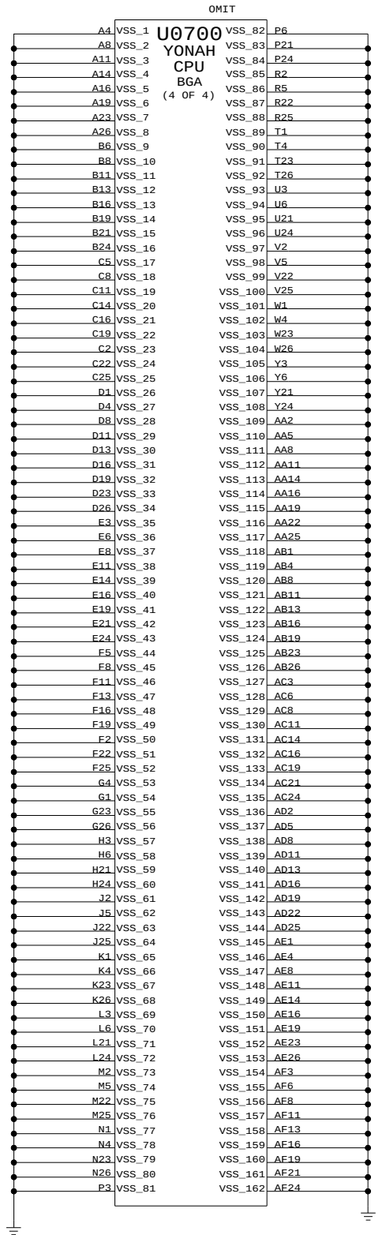

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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NONE	8	87

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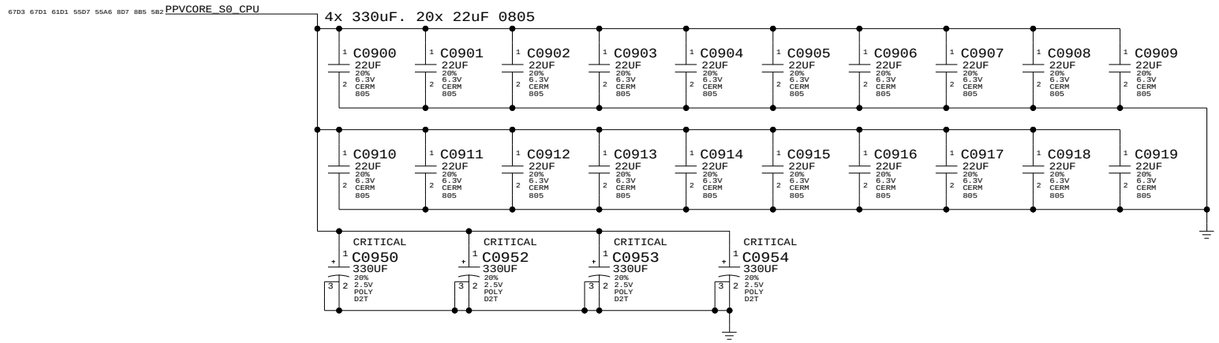
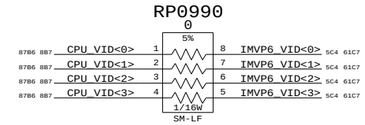
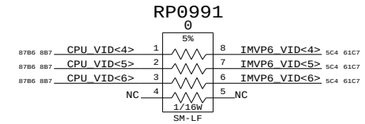
CPU VCORE HF AND BULK DECOUPLING



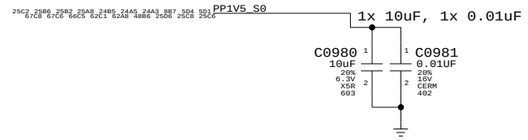
CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production

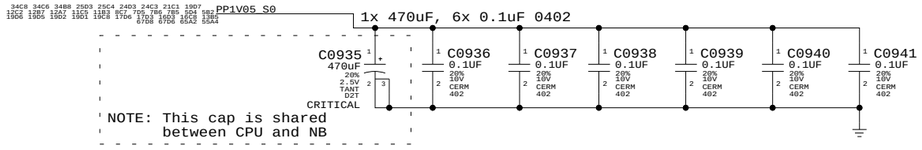




VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling



CPU Decoupling & VID

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D	051-7164	06004

SCALE	SHT	OF
NONE	9	87

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CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

67C3 67B3 67A3 66B6 66B5 66B1 65D6 65B3
54B5 26B8 26B6 26B4 25D8 25D5 25C6 25C4 25B8
21C3 20B4 20A4 19C7 19C6 17C6 14D6 14C7 5D4 5A4
25B4 25B3 24D3 24C3 24B5 24B3 23D3 23B5 23D3
22A6 22A5 22A4 22A3 22A2 22A1 21D3 21B5 21D3
62A6 61D8 61A5 60D4 60C7 58C7 58C4 57B6 54D4
82D5 82C6 82B3 82A4 79D3 79A8 71D2 67C5

PP3V3_S0

C1002 1 0.1UF 10% 16V X5R 402 2

R1006 1 10K 5% 1/16W MF-LF 402 2

R1005 1 10K 5% 1/16W MF-LF 402 2

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

OUT 7C6 CPU_THERMD_P

R1001 499 1% 1/16W MF-LF 402

IN 7C6 CPU_THERMD_N

R1002 499 1% 1/16W MF-LF 402

C1001 1 0.001UF 10% 50V CERM 402 2

THRM_CPU_DX_P
THRM_CPU_DX_N

U1001
TMP401
MSOP
CRITICAL

		1	VDD
THRM_CPU_DX_P	D+	2	
THRM_CPU_DX_N	D-	3	
THRM_ALERT_L	ALERT*/THM2*	6	
THRM_ALERT	THM*	4	
SMBUS_SMC_B_S0_SCL	SCLK	8	
SMBUS_SMC_B_S0_SDA	SDATA	7	
	GND	5	

51B5 49B5 27D3 27D2 27D1 SMBUS_SMC_B_S0_SCL TO

51B5 49B5 27D3 27D2 27D1 SMBUS_SMC_B_S0_SDA TO

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

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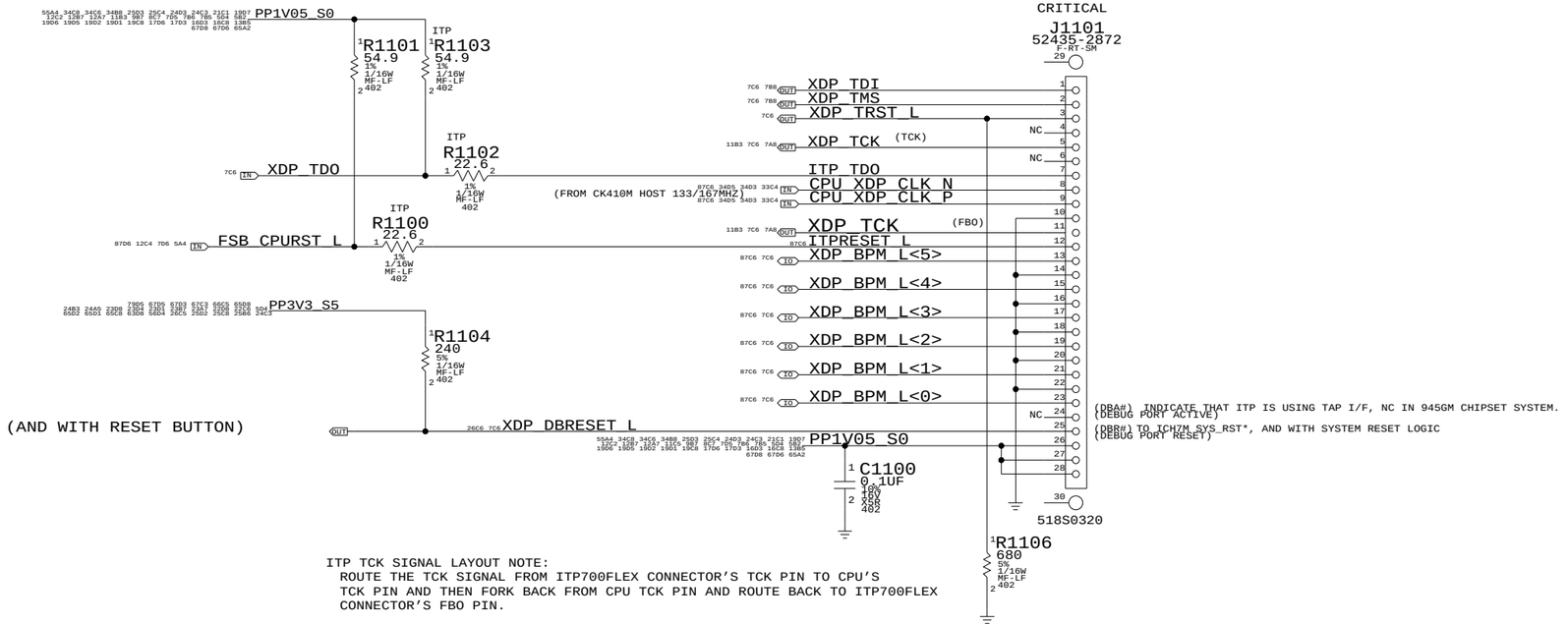
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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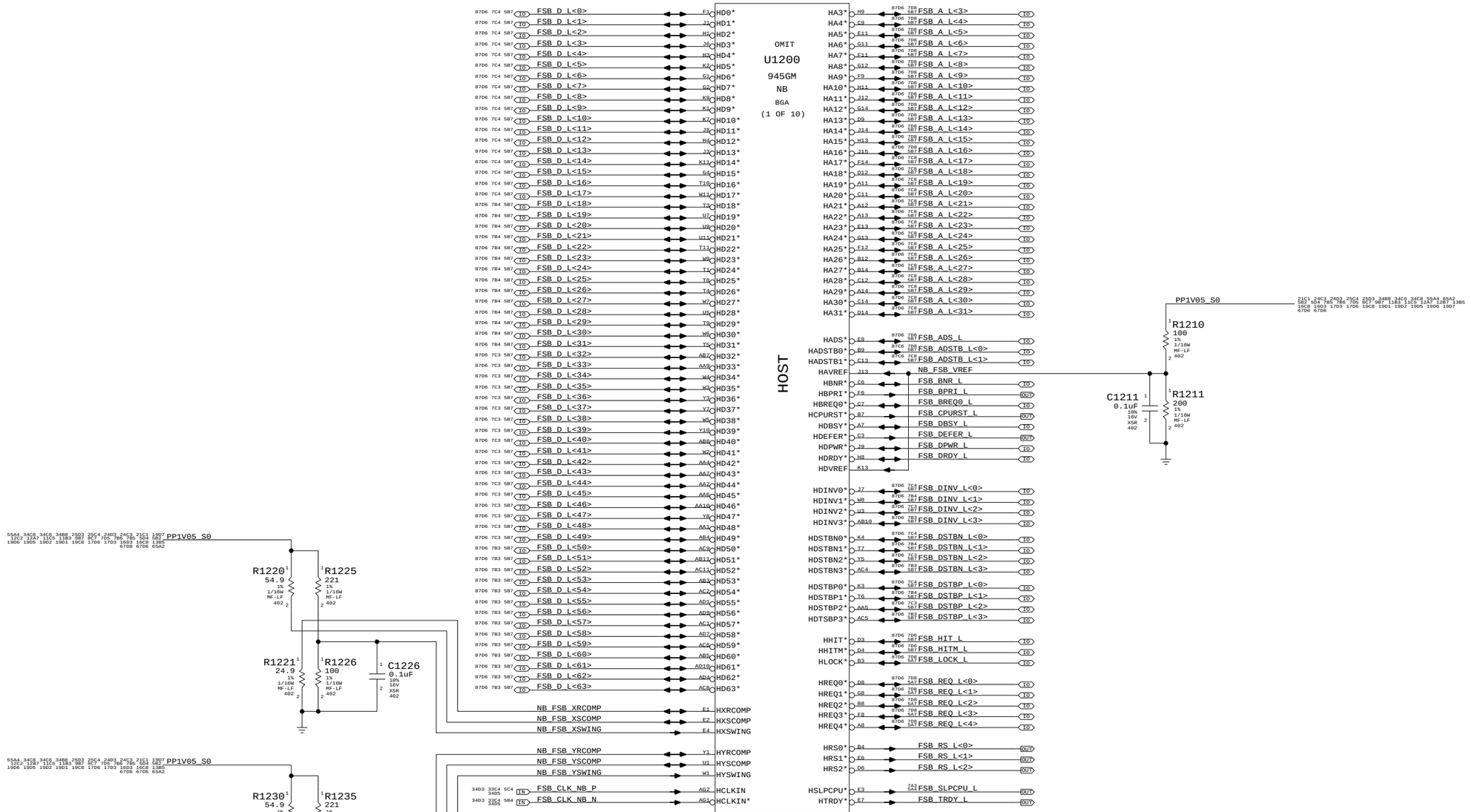

NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

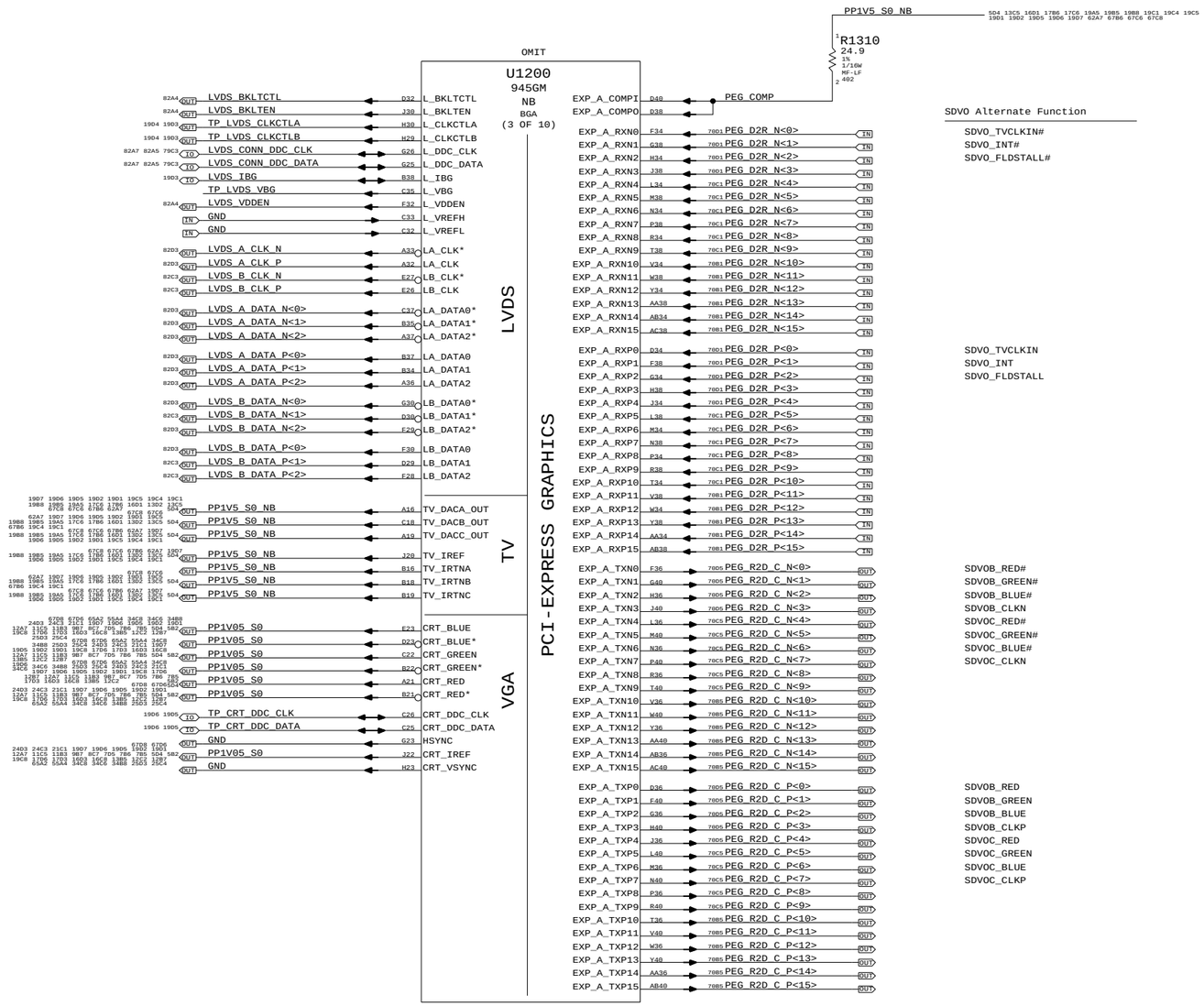
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

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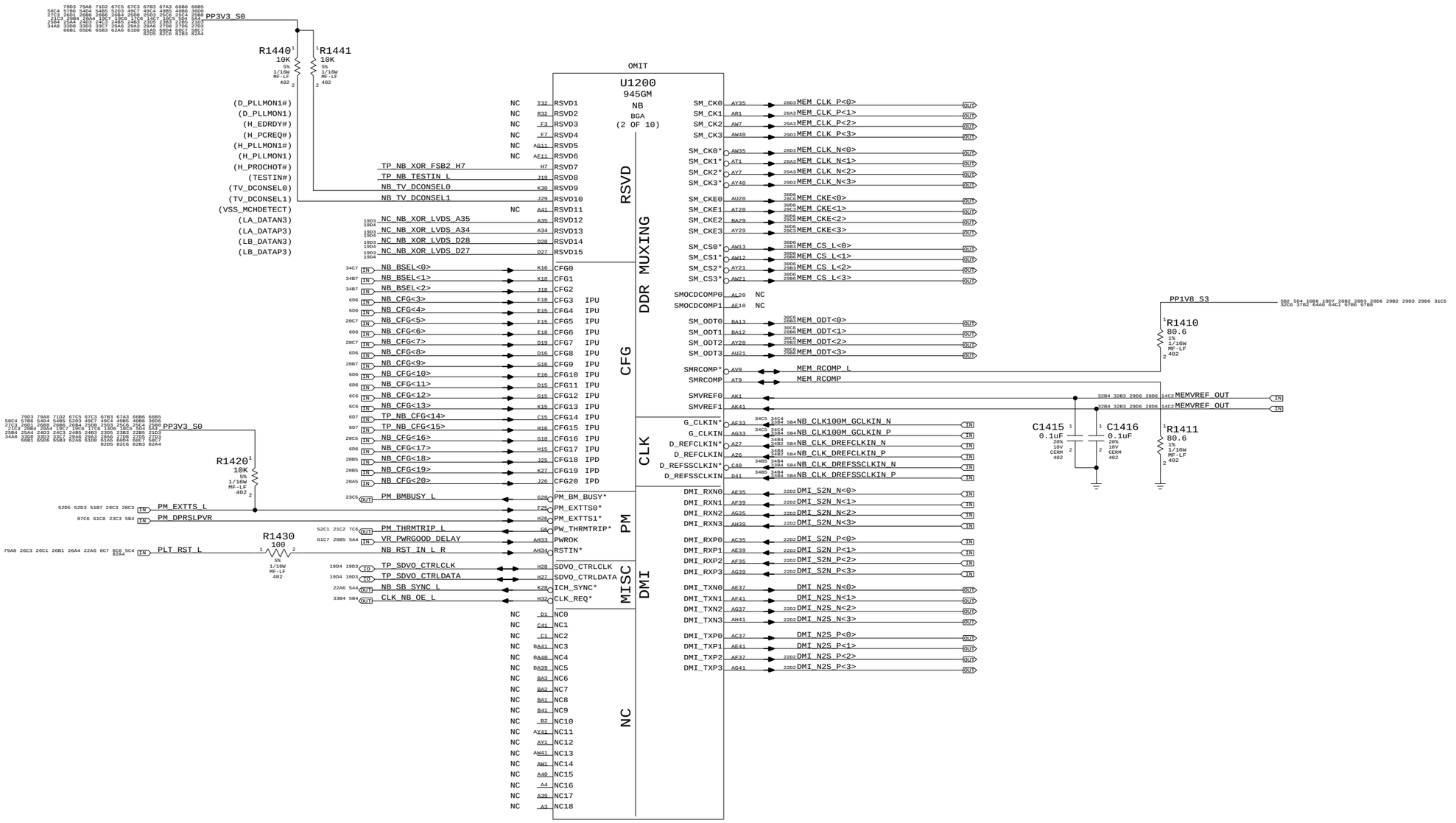

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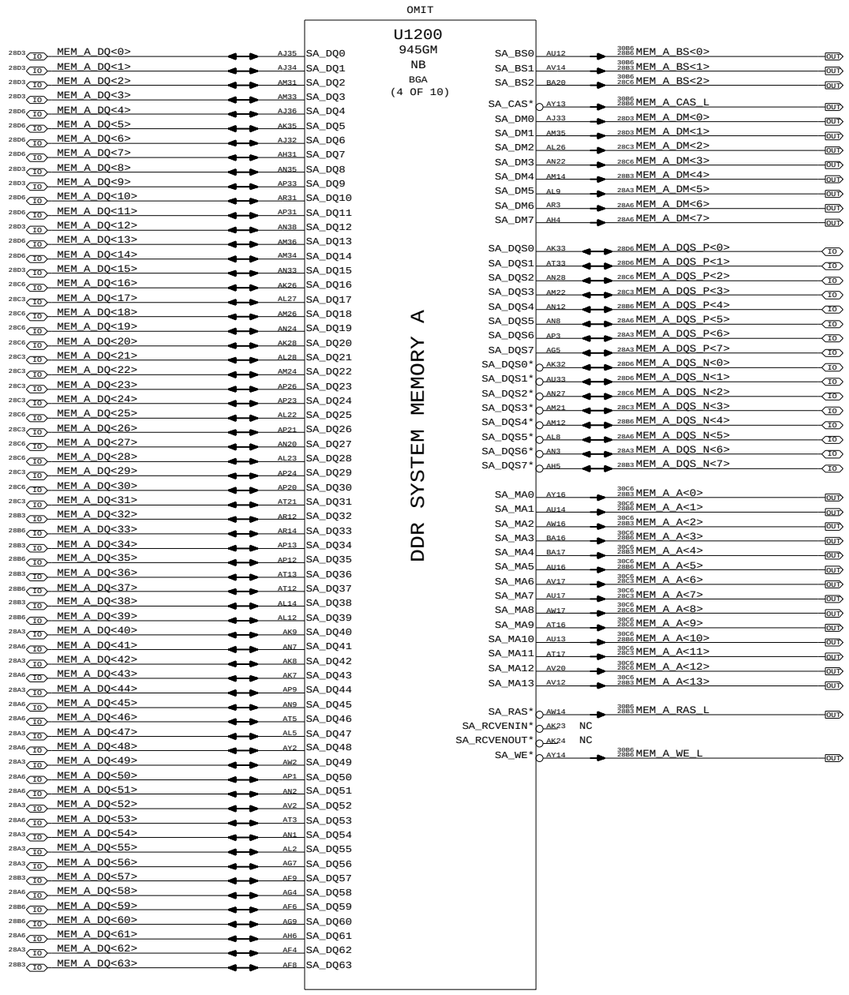

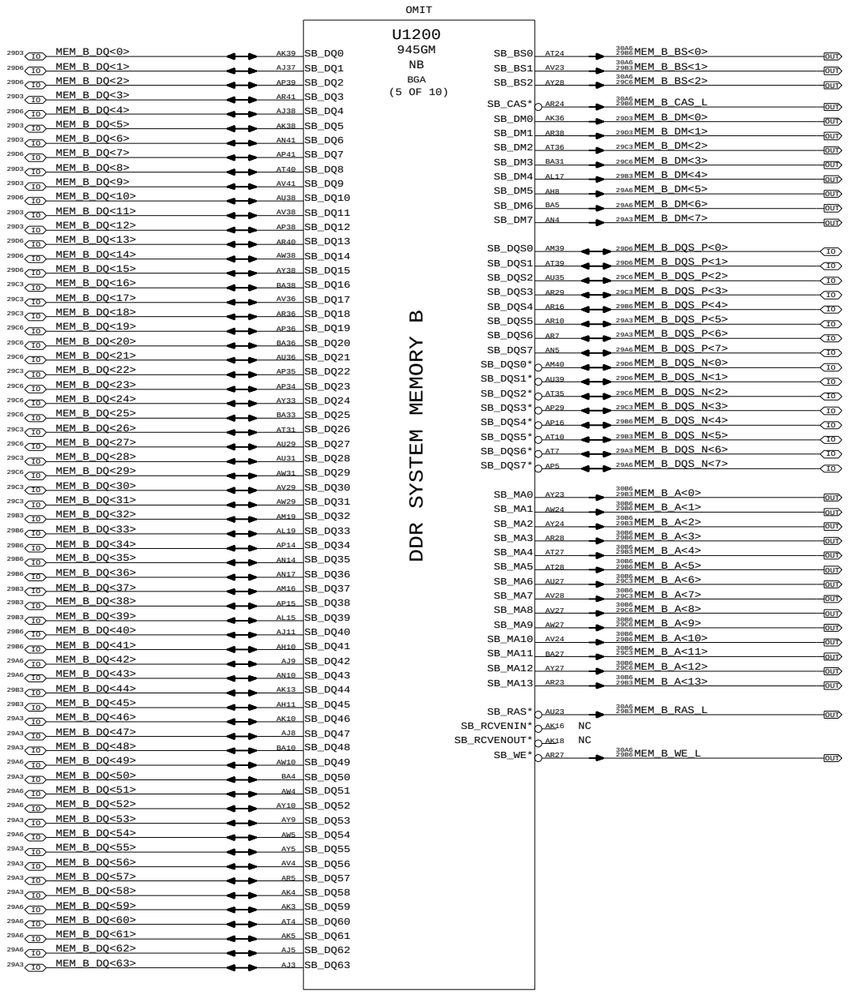

NB DDR2 Interfaces

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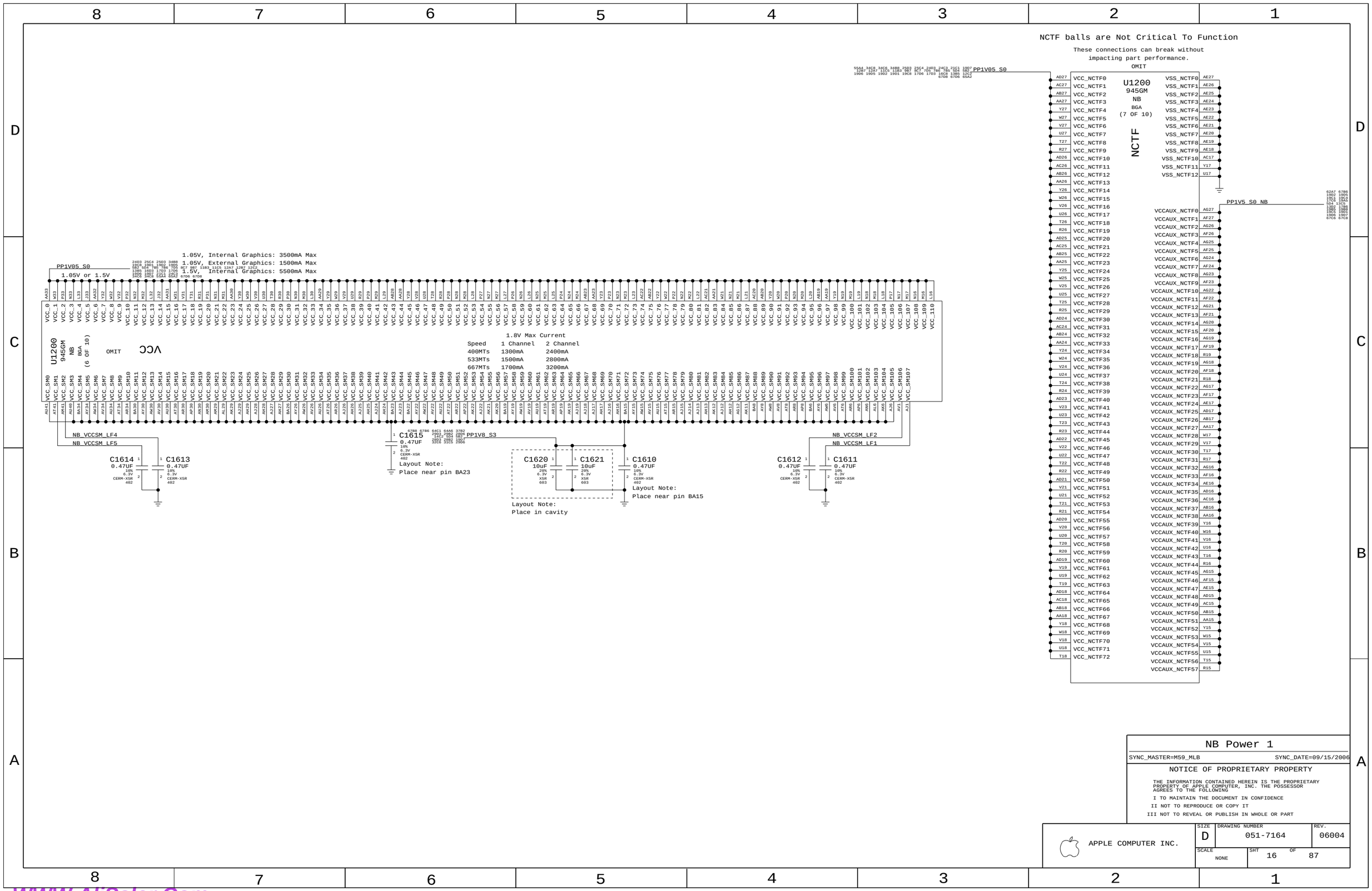
NCTF balls are Not Critical To Function
These connections can break without impacting part performance.
OMIT
U1200
945GM
NB
BGA
(7 OF 10)
NCTF
PP1V05_S0
PP1V5_S0_NB
VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110
VCC
1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.05V, Internal Graphics: 5500mA Max
1.8V Max Current
Speed 1 Channel 2 Channel
400MTs 1300mA 2400mA
533MTs 1500mA 2800mA
667MTs 1700mA 3200mA
VCC_NCTF0 VCC_NCTF1 VCC_NCTF2 VCC_NCTF3 VCC_NCTF4 VCC_NCTF5 VCC_NCTF6 VCC_NCTF7 VCC_NCTF8 VCC_NCTF9 VCC_NCTF10 VCC_NCTF11 VCC_NCTF12 VCC_NCTF13 VCC_NCTF14 VCC_NCTF15 VCC_NCTF16 VCC_NCTF17 VCC_NCTF18 VCC_NCTF19 VCC_NCTF20 VCC_NCTF21 VCC_NCTF22 VCC_NCTF23 VCC_NCTF24 VCC_NCTF25 VCC_NCTF26 VCC_NCTF27 VCC_NCTF28 VCC_NCTF29 VCC_NCTF30 VCC_NCTF31 VCC_NCTF32 VCC_NCTF33 VCC_NCTF34 VCC_NCTF35 VCC_NCTF36 VCC_NCTF37 VCC_NCTF38 VCC_NCTF39 VCC_NCTF40 VCC_NCTF41 VCC_NCTF42 VCC_NCTF43 VCC_NCTF44 VCC_NCTF45 VCC_NCTF46 VCC_NCTF47 VCC_NCTF48 VCC_NCTF49 VCC_NCTF50 VCC_NCTF51 VCC_NCTF52 VCC_NCTF53 VCC_NCTF54 VCC_NCTF55 VCC_NCTF56 VCC_NCTF57 VCC_NCTF58 VCC_NCTF59 VCC_NCTF60 VCC_NCTF61 VCC_NCTF62 VCC_NCTF63 VCC_NCTF64 VCC_NCTF65 VCC_NCTF66 VCC_NCTF67 VCC_NCTF68 VCC_NCTF69 VCC_NCTF70 VCC_NCTF71 VCC_NCTF72
VSS_NCTF0 VSS_NCTF1 VSS_NCTF2 VSS_NCTF3 VSS_NCTF4 VSS_NCTF5 VSS_NCTF6 VSS_NCTF7 VSS_NCTF8 VSS_NCTF9 VSS_NCTF10 VSS_NCTF11 VSS_NCTF12
VCCAUX_NCTF0 VCCAUX_NCTF1 VCCAUX_NCTF2 VCCAUX_NCTF3 VCCAUX_NCTF4 VCCAUX_NCTF5 VCCAUX_NCTF6 VCCAUX_NCTF7 VCCAUX_NCTF8 VCCAUX_NCTF9 VCCAUX_NCTF10 VCCAUX_NCTF11 VCCAUX_NCTF12 VCCAUX_NCTF13 VCCAUX_NCTF14 VCCAUX_NCTF15 VCCAUX_NCTF16 VCCAUX_NCTF17 VCCAUX_NCTF18 VCCAUX_NCTF19 VCCAUX_NCTF20 VCCAUX_NCTF21 VCCAUX_NCTF22 VCCAUX_NCTF23 VCCAUX_NCTF24 VCCAUX_NCTF25 VCCAUX_NCTF26 VCCAUX_NCTF27 VCCAUX_NCTF28 VCCAUX_NCTF29 VCCAUX_NCTF30 VCCAUX_NCTF31 VCCAUX_NCTF32 VCCAUX_NCTF33 VCCAUX_NCTF34 VCCAUX_NCTF35 VCCAUX_NCTF36 VCCAUX_NCTF37 VCCAUX_NCTF38 VCCAUX_NCTF39 VCCAUX_NCTF40 VCCAUX_NCTF41 VCCAUX_NCTF42 VCCAUX_NCTF43 VCCAUX_NCTF44 VCCAUX_NCTF45 VCCAUX_NCTF46 VCCAUX_NCTF47 VCCAUX_NCTF48 VCCAUX_NCTF49 VCCAUX_NCTF50 VCCAUX_NCTF51 VCCAUX_NCTF52 VCCAUX_NCTF53 VCCAUX_NCTF54 VCCAUX_NCTF55 VCCAUX_NCTF56 VCCAUX_NCTF57
NB_VCCSM_LF4
NB_VCCSM_LF5
NB_VCCSM_LF2
NB_VCCSM_LF1
C1614 0.47UF 10% 6.3V CERM-X5R 402
C1613 0.47UF 10% 6.3V CERM-X5R 402
C1615 0.47UF 10% 6.3V CERM-X5R 402
C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
C1610 0.47UF 10% 6.3V CERM-X5R 402
C1612 0.47UF 10% 6.3V CERM-X5R 402
C1611 0.47UF 10% 6.3V CERM-X5R 402
Layout Note:
Place near pin BA23
Layout Note:
Place in cavity
Layout Note:
Place near pin BA15
NB Power 1
SYNC_MASTER=M59_MLB
SYNC_DATE=09/15/2006
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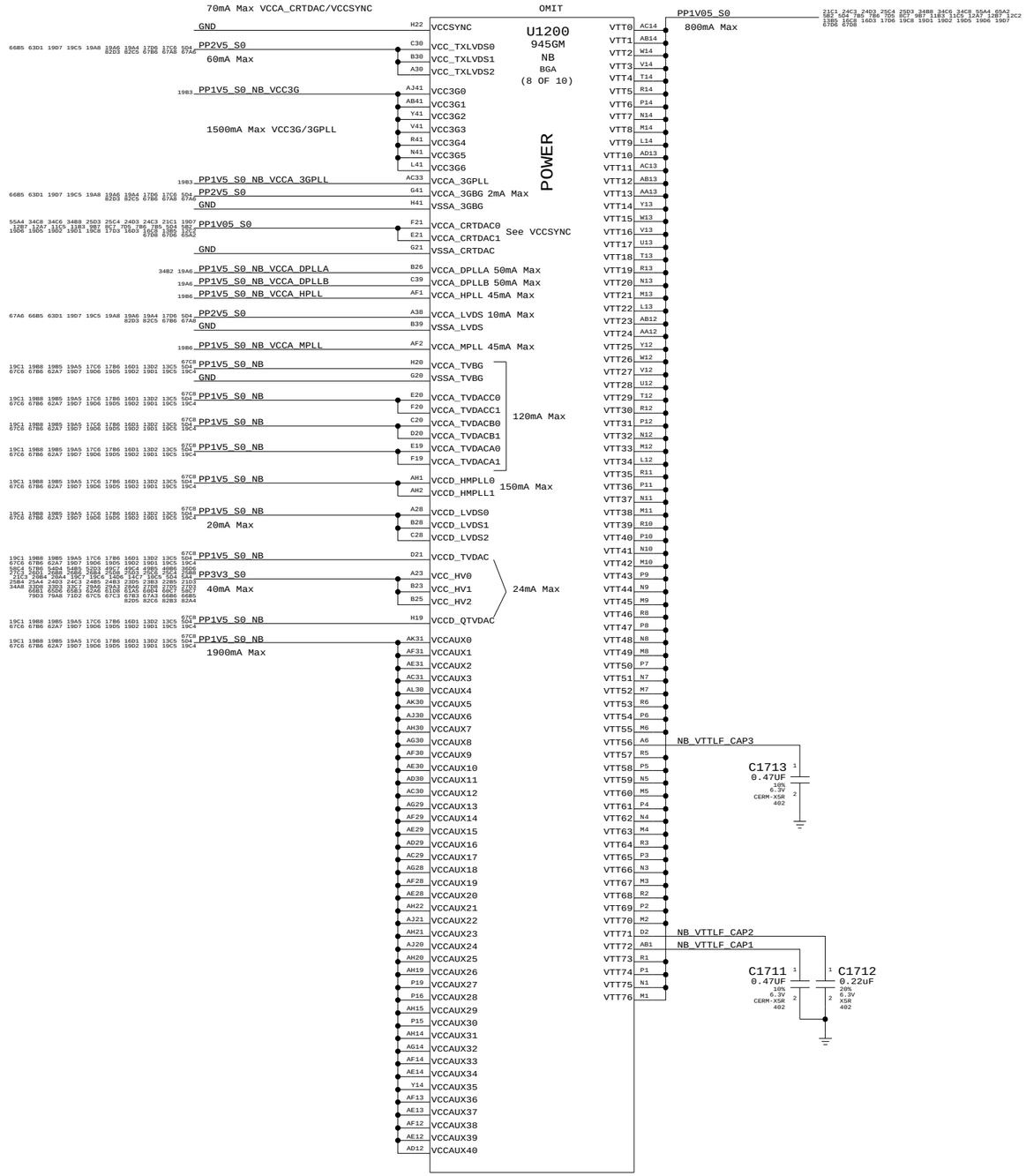

SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006

NB Power 2

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NONE	17	87

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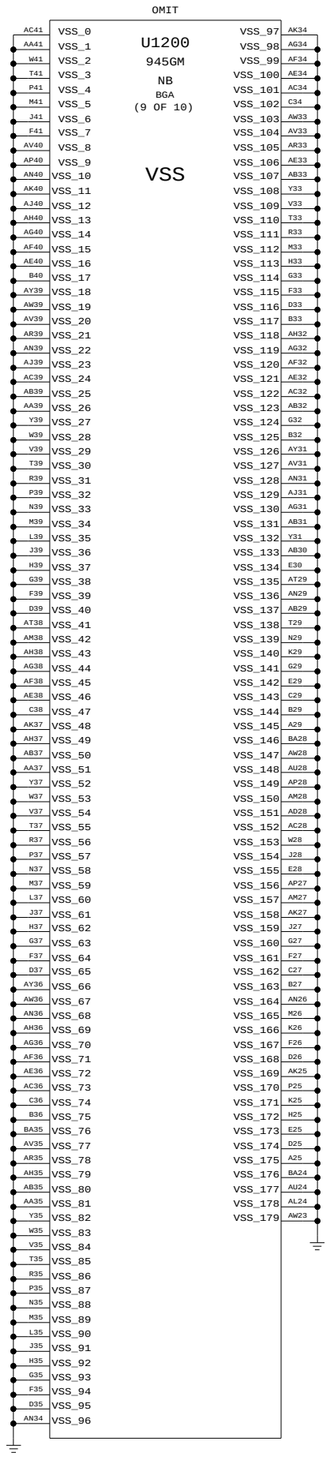

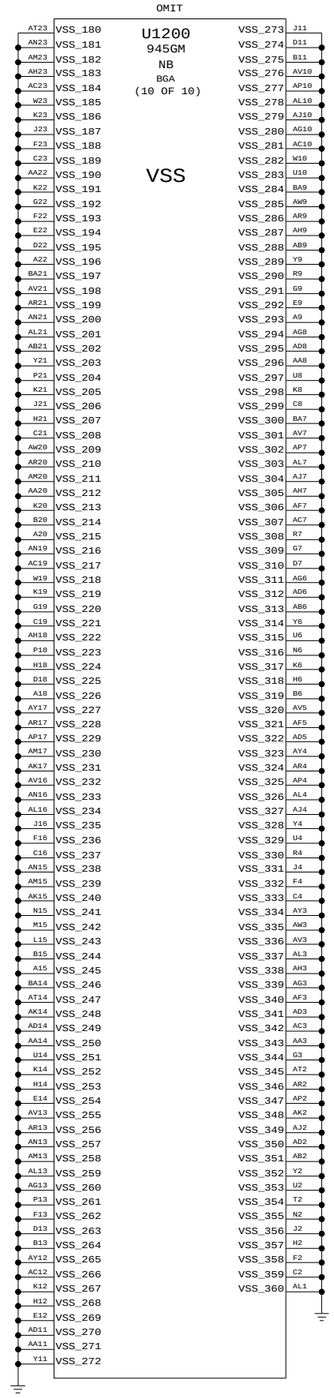

NB Grounds

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Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?
- PP1V05_S0 — 10mA Max?
- PP1V05_S0 — 1500mA Max
- PP1V05_S0 — 800mA Max
- PP1V05_S0 — 7mA Max

3674mA Max
- PP1V5_S0_NB — 7mA Max
- PP1V5_S0_NB — 1500mA Max
- PP1V5_S0_NB — 7mA Max
- PP1V5_S0_NB — 100mA Max
- PP1V5_S0_NB — 24mA Max
- PP1V5_S0_NB — 150mA Max
- PP1V5_S0_NB — 190mA Max

3200mA Max
- PP1V8_S3 — 3200mA Max

132mA Max
- GND — 70mA Max
- PP2V5_S0 — 60mA Max
- PP2V5_S0 — 2mA Max

40mA Max?
- PP3V3_S0 — 40mA Max

PP1V05_S0 → PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, GND, GND

PP1V5_S0_NB → PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB

TP_CRT_DDC_CLK — MAKE_BASE=TRUE → TP_CRT_DDC_CLK

TP_CRT_DDC_DATA — MAKE_BASE=TRUE → TP_CRT_DDC_DATA

TP_LVDS_CLKCTLA — MAKE_BASE=TRUE → TP_LVDS_CLKCTLA

TP_LVDS_CLKCTLB — MAKE_BASE=TRUE → TP_LVDS_CLKCTLB

NC_NB_XOR_LVDS_A34 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_A34

NC_NB_XOR_LVDS_A35 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_A35

NC_NB_XOR_LVDS_D27 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_D27

NC_NB_XOR_LVDS_D28 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_D28

TP_SDVO_CTRLCLK — MAKE_BASE=TRUE → TP_SDVO_CTRLCLK

TP_SDVO_CTRLDATA — MAKE_BASE=TRUE → TP_SDVO_CTRLDATA

LVDS IBG

R1990 1.5K 1% 1/16W MF-LF 402 — GND, GND

PP1V05_S0 → PP1V05_S0, GND, PP1V5_S0_NB

(MCH CRTDAC ANALOG 2.5V PWR): PP1V05_S0, GND

(MCH H/V SYNC 2.5V PWR): GND

(MCH TVDAC DEDICATED PWR 1.5V): PP1V5_S0_NB

(MCH TVDAC DIGITAL QUIET 1.5V PWR): PP1V5_S0_NB

(MCH TV OUT CHANNEL A 3.3V PWR): PP1V5_S0_NB

(MCH TV OUT CHANNEL B 3.3V PWR): PP1V5_S0_NB

(MCH TV OUT CHANNEL C 3.3V PWR): PP1V5_S0_NB

(MCH TV DAC BAND GAP 3.3V PWR): PP1V5_S0_NB

GND

GMCH CORE PWR 1.05V BYPASS

PP1V05_S0 — 1500mA Max

CRITICAL
- C1900 470uF 20% 2.5V TANT D2T
- C1902 10uF 20% 6.3V X5R 603
- C1903 10uF 20% 6.3V X5R 603
- C1904 1uF 10% 6.3V CERM 402
- C1905 0.22uF 20% 6.3V X5R 402
- C1906 0.22uF 20% 6.3V X5R 402
- C1907 0.22uF 20% 6.3V X5R 402

MCH VTT BYPASS (MCH FSB 1.05V PWR)

PP1V05_S0 — 800mA Max

- C1965 4.7uF 20% 6.3V CERM 603
- C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

PP3V3_S0 — 40mA Max (SHARE C0940 470UF)

- C1967 0.22uF 20% 6.3V X5R 402

Layout Note: Place on the edge

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

PP2V5_S0 — 2mA Max

- C1914 10uF 20% 6.3V X5R 603
- C1915 0.1uF 20% 10V CERM 402
- C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

PP1V5_S0_NB — 1900mA Max

- C1918 0.1uF 20% 10V CERM 402

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)

PP1V5_S0_NB_VCC3G — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V

- C1971 10uF 20% 6.3V X5R 603
- C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

1500mA Max

GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)

PP1V5_S0_NB → L1934 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_HPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 45mA Max

- C1934 22UF 20% 6.3V CERM 805
- C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

PP1V5_S0_NB → L1936 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_MPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 45mA Max

- C1936 22UF 20% 6.3V CERM 805
- C1937 0.1uF 20% 10V CERM 402

1500mA Max

L1970 91nH 1210

Layout Note: Place L and C close to MCH

- C1970 220UF 20% 2.5V POLY CASE-B2

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)

PP1V5_S0_NB → L1975 1.0UH-220MA-0.12-OHM 0805 — PP1V5_S0_NB_3GPLL_F — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V

R1975 0.51 1% 1/16W MF-LF 402

PP1V5_S0_NB_VCCA_3GPLL — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V

- C1975 10uF 20% 6.3V X5R 603
- C1976 0.1uF 20% 10V CERM 402

GND

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

1500mA Max

GMCH VCCA_DPLLA FILTER (CRT/TVOUT PLL 1.5V PWR)

NO STUFF R1953 0 5% 1/16W MF-LF 402

PP1V5_S0_NB_VCCA_DPLLA — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 50MA MAX

GMCH VCCA_DPLLB FILTER (LVDS PLL 1.5V PWR)

NO STUFF R1954 0 5% 1/16W MF-LF 402

PP1V5_S0_NB_VCCA_DPLLB — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 50MA MAX

CRITICAL U1900 TPS73115 SOT23-5 (IN, OUT, EN, NR/FB, GND)

PP2V5_S0 → C1950 1uF 10% 6.3V CERM 402

PP1V5_S0_NB_DPLL → C1951 0.01uF 10% 16V CERM 402; C1952 10uF 20% 6.3V X5R 603

TPS73115_NR

C1953 0.1uF 20% 10V CERM 402; C1954 0.1uF 20% 10V CERM 402

MCH VCC_TXLVDS BYPASS (MCH LVDS TRANSMITTER 2.5V PWR)

PP2V5_S0 — 60MA MAX

- C1990 4.7UF 20% 6.3V CERM 603
- C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)

PP1V5_S0_NB — 20MA MAX

- C1992 10uF 20% 6.3V X5R 603
- C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS (MCH LVDS ANALOG 2.5V PWR)

PP2V5_S0 — 10MA MAX

- C1994 0.01UF 20% 16V CERM 402
- C1995 0.1uF 20% 10V CERM 402

GND

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NB_CFG<17>	RESERVED

PP3V3_S0
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

14C6 NB_CFG<18>
Internal pull-down

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

PP3V3_S0
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

14C6 NB_CFG<19>
Internal pull-down

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

945 External Design Spec says reserved

PP3V3_S0
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

14B6 NB_CFG<20>
Internal pull-down

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

PROBABLY NOT NEEDED

NB Config Straps

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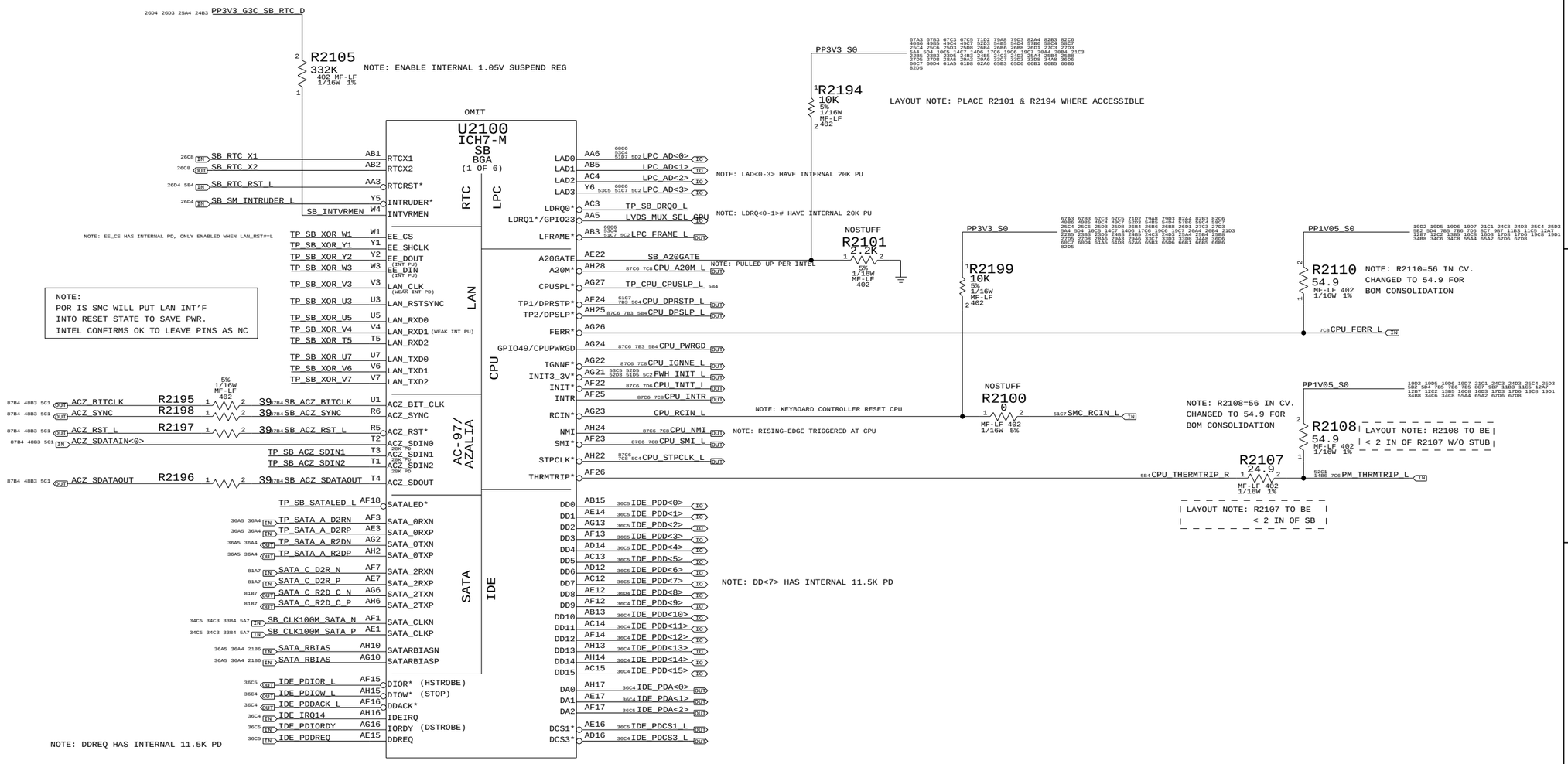

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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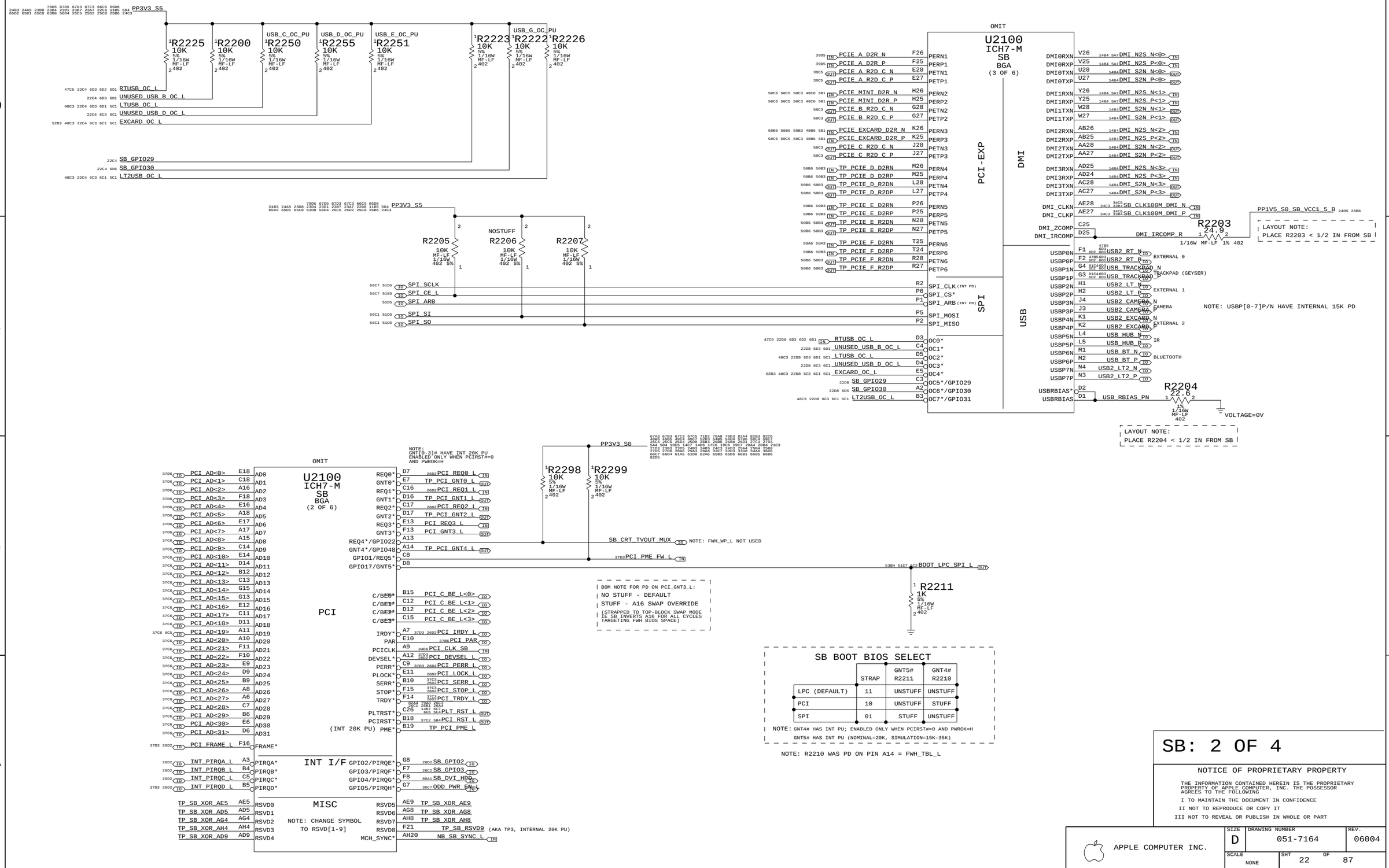

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

PP3V3_S0

PP3V3_S5

RP2300 10K 5% 1/16W SM-LF

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMBUS_SB_SCL → SMBCLK C22
SMBUS_SB_SDA → SMBDATA B22
SMB_LINK_ALERT_L → LINKALERT* A26
SMLINK<0> → SMLINK0 B25
SMLINK<1> → SMLINK1 A25
NOT USED
PM_RI_L → RI* A28
SB_SPKR → SPKR (INT WEAK PD) A19
PM_SUS_STAT_L → SUS_STAT* A27
PM_SYSRST_L → SYS_RST* A22
PM_BMBUSY_L → GPIO0/BM_BUSY* AB18
SMB_ALERT_L → GPIO11/SMBALERT* B23
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L → GPIO18/STPPCI* AC20
PM_STPCPU_L → GPIO20/STPCPU* AF21
SB_GPIO26 → GPIO26 A21
BIOS_REC → GPIO27 B21
FWH_MFG_MODE → GPIO28 E23
PM_CLKRUN_L → GPIO32/CLKRUN* AG18
GPU_D3COLD_RESET_L → GPIO33/AZ_DOCK_EN* AC19
TP_AZ_DOCK_RST_L → GPIO34/AZ_DOCK_RST* U2
PCIE_WAKE_L → WAKE* F20
INT_SERIRQ → SERIRQ AH21
PM_THRM_L → THRM* AF20
VR_PWRGD_CK410 → VRMPWRGD AD22
TP_SB_GPIO6 → GPIO6 AC21
SMC_RUNTIME_SCI_L → GPIO7 AC18
SMC_EXTSMI_L → GPIO8 E21

SMB

SATA GPIO
GPIO21/SATA0GP → AF19 SB_GPIO21 → R2302 100
GPIO19/SATA1GP → AH18 SB_GPIO19 → R2303 100
GPIO36/SATA2GP → AH19
GPIO37/SATA3GP → AE19 SB_GPIO37 → R2305 100
SATA_C_DET_L

CLKS
CLK14 → AC1 SB_CLK14P3M_TIMER
CLK48 → B2 SB_CLK48M_USBCTLR
SUSCLK → C20 TP_SB_SUS_CLK

SYS GPIO / PWR MNGT
SLP_S3* → PM_SLP_S3_L
SLP_S4* → B24 PM_SLP_S4_L
SLP_S5* → D23 PM_SLP_S5_L
PWROK → F22 PM_SB_PWROK
GPIO16/DPRSLPVR → AA4 PM_DPRSLPVR
TP0/BATLOW* → AC22 PM_BATLOW_L
PWRBTN* (INT 20K PU) → C21 PM_PWRBTN_L
LAN_RST* → C23 PM_LAN_ENABLE
RSMRST* → C19 PM_RSMRST_L
NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR

GPIO
GPIO9 → E20 SMS_INT_L
GPIO10 → A20 SMC_SB_NMI
DEF=GPI GPIO12 → F19 LAN_ENERGY_DET
GPIO13 → E19 SMC_WAKE_SCI_L
DEF=GPI GPIO14 → R4 IDE_RESET_L
GPIO15 → E22 SV_SET_UP
GPIO24 → R3 CRB_SV_DET
GPIO25 → D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 → AD21 SB_CLK100M_SATA_OE_L
GPIO36 → AD20 SB_GPUVCORE_DISABLE_L
DEF=GPI GPIO39 → AE20 SATA_C_PWR_EN_L

R2399 100K 5% 1/16W 402 MF-LF

PP3V3_S5

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 1/16W 402 MF-LF 5%

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

PP3V3_S0

R2388 10K 5% 1/16W MF-LF 402

SATA_C_PWR_EN_L

PP3V3_S5

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE
BIOS_REC

SB: 3 OF 4

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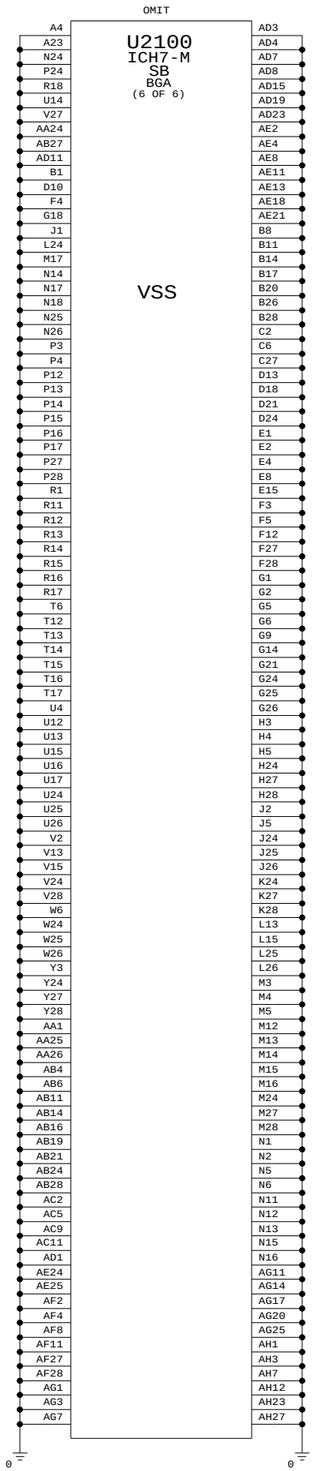

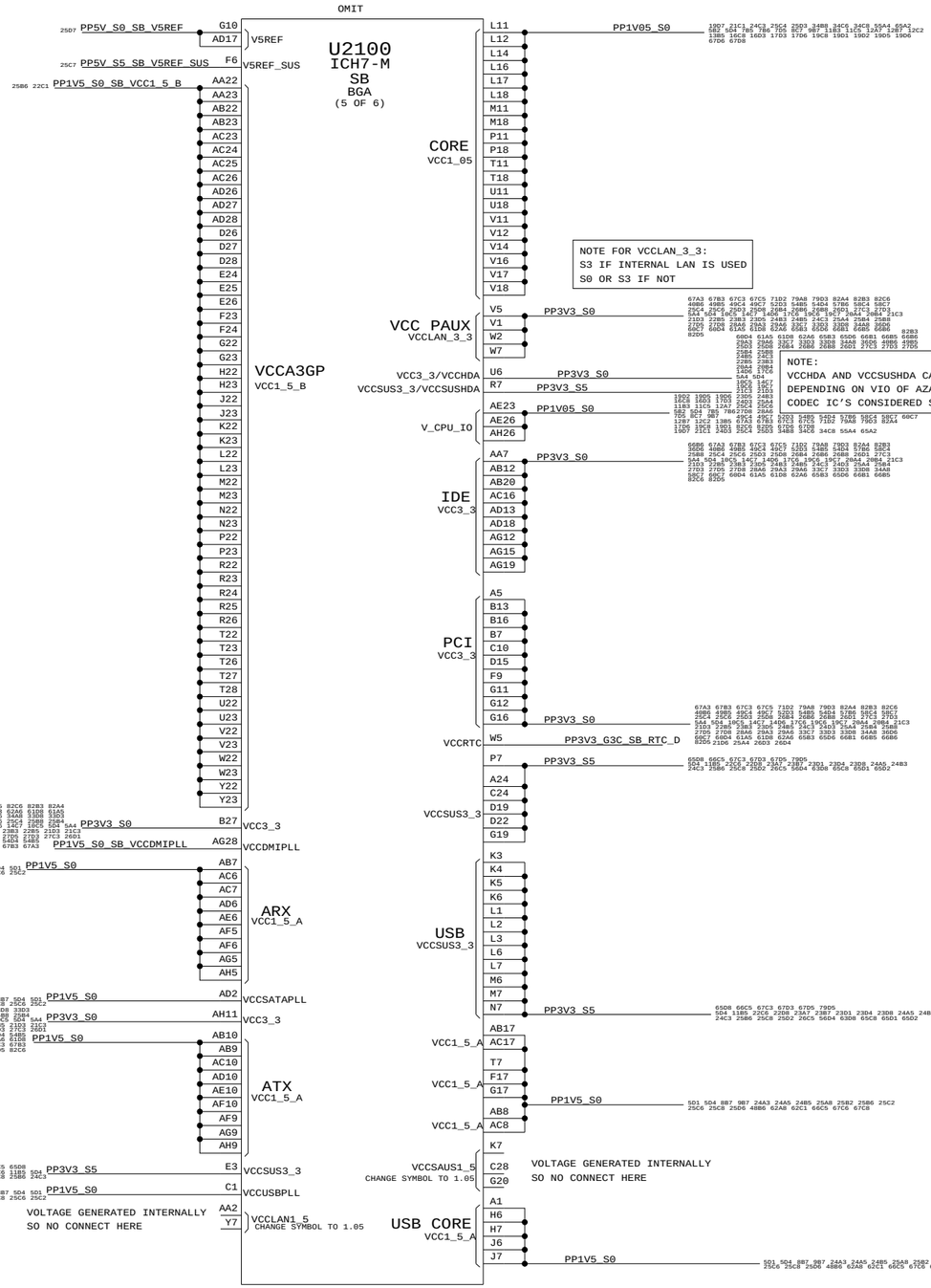

SB: 4 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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PP3V3_S0
PP5V_S0
R2502
100
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503
0.1UF
10%
16V
X5R
402
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PP3V3_S5
PP5V_S5
R2501
10
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504
0.1UF
10%
16V
X5R
402
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PP1V5_S0
L2500
100-OHM-EMI
SM-3
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500
220UF
20%
2V
POLY
CASE-B2
C2505
0.1UF
10%
16V
X5R
402
C2506
0.1UF
10%
16V
X5R
402
C2507
0.1UF
10%
16V
X5R
402
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28

PP1V5_S0
C2511
0.1UF
10%
16V
X5R
402
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5

PP1V5_S0
C2517
0.1UF
10%
16V
X5R
402
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2

PP3V3_S0
C2513
0.1UF
10%
16V
X5R
402
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11

PP1V5_S0
C2514
1UF
10%
6.3V
CERM
402
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9

PP3V3_S5
C2520
0.1UF
10%
16V
X5R
402
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB

PP3V3_S0
C2509
0.1UF
10%
16V
X5R
402
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB

PP1V5_S0
C2515
0.1UF
10%
16V
X5R
402
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB

PP1V5_S0
R2500
1
1/10W 5%
MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L2507
0.28-OHM
1206
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2501
0.01UF
10%
16V
CERM
402
C2508
10UF
20%
6.3V
X5R
603
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

PP1V05_S0
C2518
0.1UF
10%
16V
X5R
402
C2502
1UF
10%
6.3V
CERM
402
C2516
330UF
20%
2.5V
POLY
CASE-C2
PLACEHOLDER
FOR 270UF
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)

PP3V3_S5
C2531
0.1UF
10%
16V
X5R
402
C2534
0.1UF
10%
16V
X5R
402
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB

PP3V3_S0
C2519
0.1UF
10%
16V
X5R
402
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V1,
V5, W2, OR W7

PP3V3_S5
C2533
0.1UF
10%
16V
X5R
402
C2532
0.1UF
10%
16V
X5R
402
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB

PP3V3_S0
C2521
0.1UF
10%
16V
X5R
402
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6

PP1V5_S0
C2510
0.1UF
10%
16V
X5R
402
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB

PP1V05_S0
C2523
0.1UF
10%
16V
X5R
402
C2522
0.1UF
10%
16V
X5R
402
C2524
4.7UF
20%
6.3V
CERM
603
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB

PP1V5_S0
C2512
0.1UF
10%
16V
X5R
402
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... J7

PP3V3_S0
C2525
0.1UF
10%
16V
X5R
402
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7 ... AG19

PP3V3_S0
C2526
0.1UF
10%
16V
X5R
402
C2527
0.1UF
10%
16V
X5R
402
C2528
0.1UF
10%
16V
X5R
402
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16

PP3V3_G3C_SB_RTC_D
C2530
0.1UF
10%
16V
X5R
402
C2529
0.1UF
10%
16V
X5R
402
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB

SB: 4 OF 4

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 25 OF 87	

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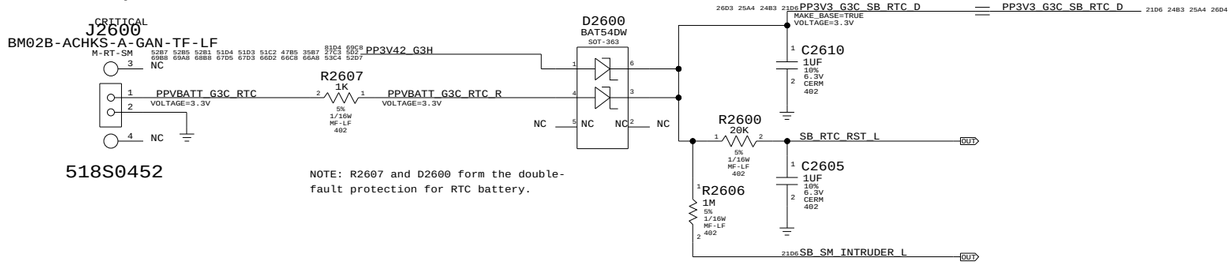
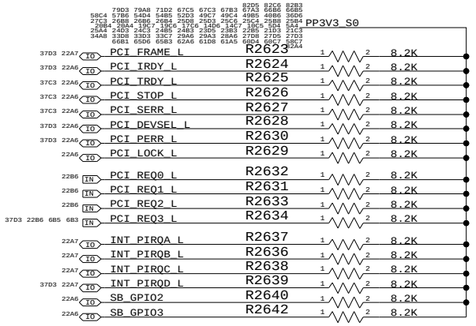
RTC Battery Connector



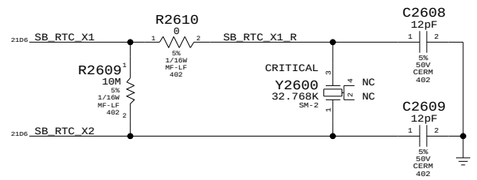
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.

PCI Pull-ups

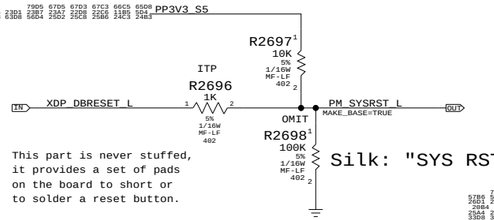


Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit



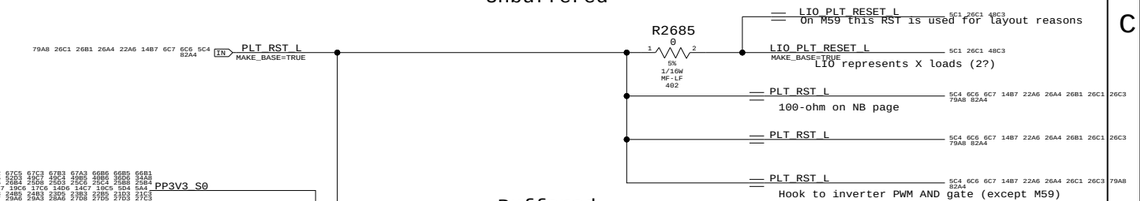
Silk: "SYS RST"



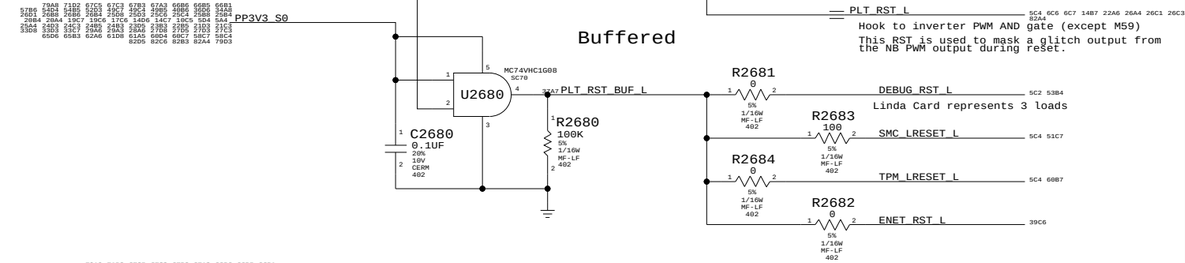
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Platform Reset Connections

Unbuffered

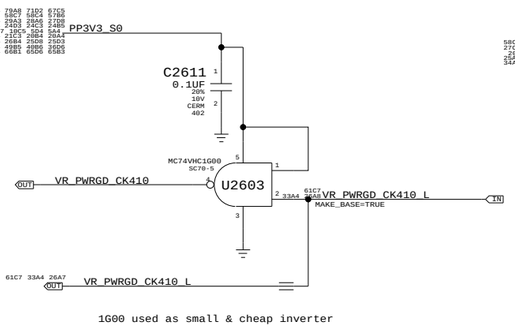


Buffered

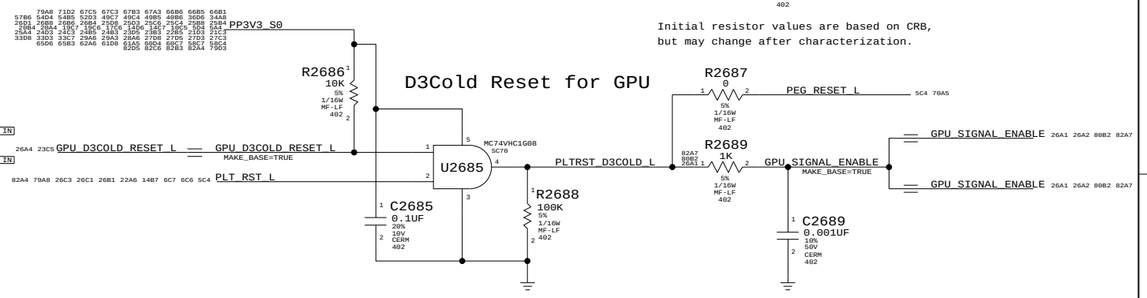


Initial resistor values are based on CRB, but may change after characterization.

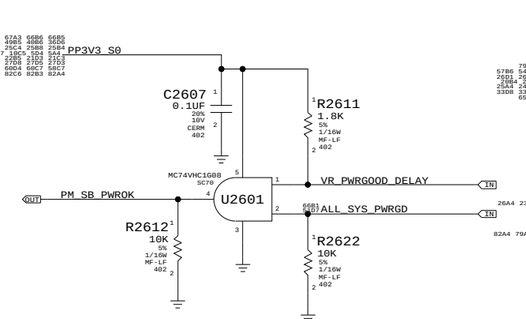
1G00 used as small & cheap inverter



D3Cold Reset for GPU



PM_SB_PWROK Delay



SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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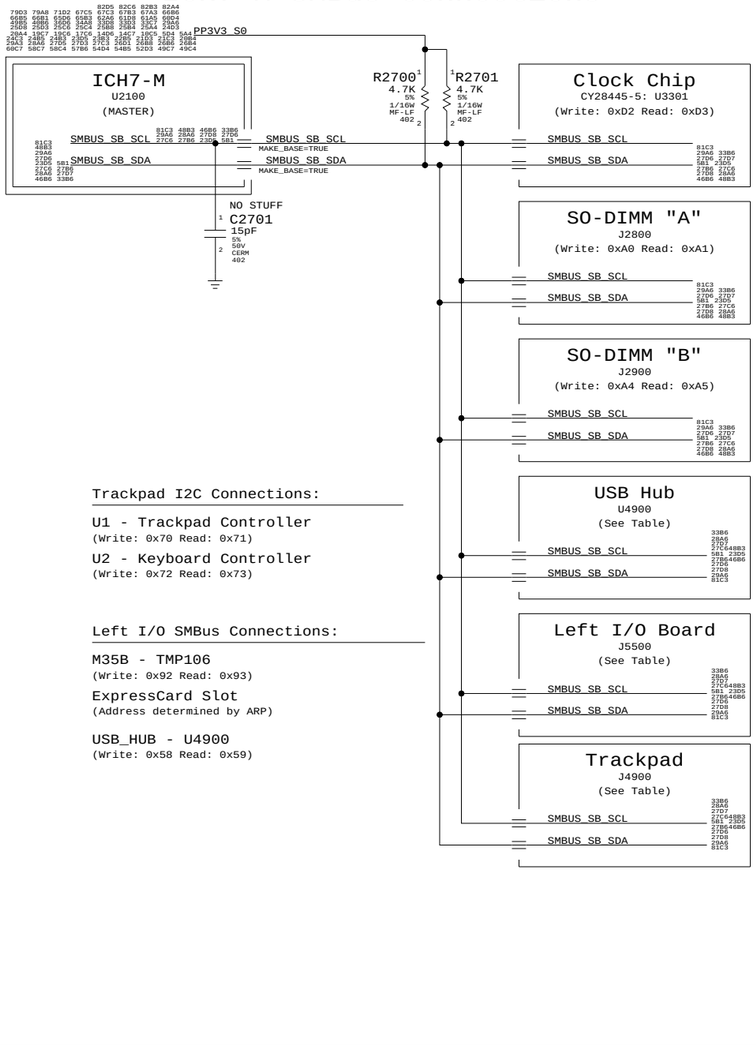
ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

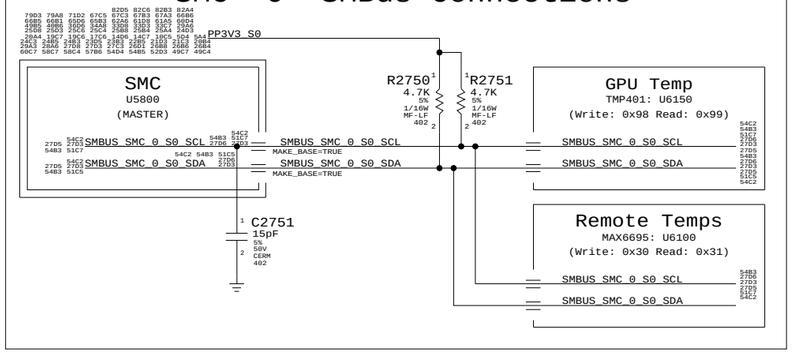
Left I/O SMBus Connections:

M35B - TMP106
(Write: 0x92 Read: 0x93)

ExpressCard Slot
(Address determined by ARP)

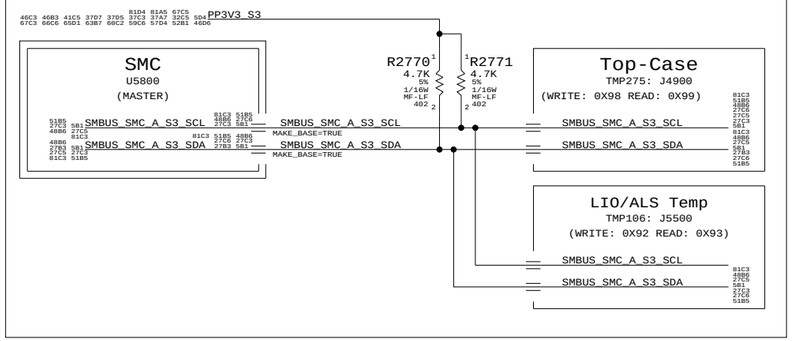
USB_HUB - U4900
(Write: 0x58 Read: 0x59)

SMC "0" SMBus Connections

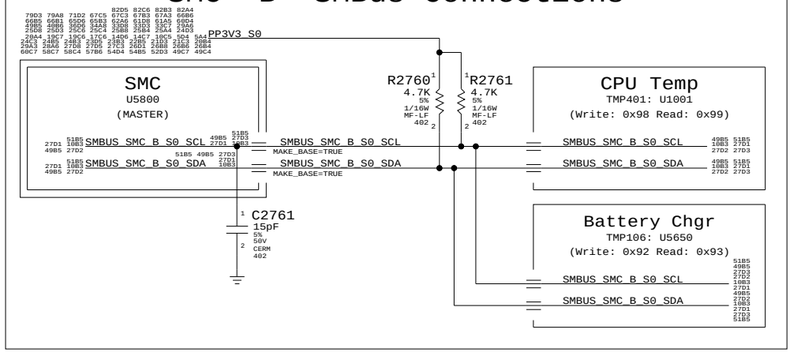


SMC "A" SMBus Connections

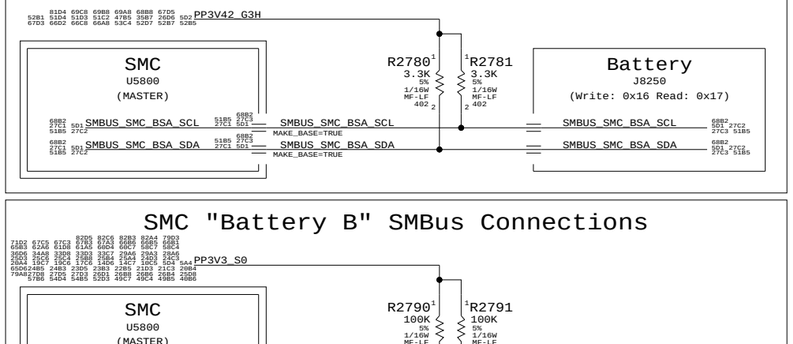
NOTE: SMC RMT bus remains powered and may be active in S3 state



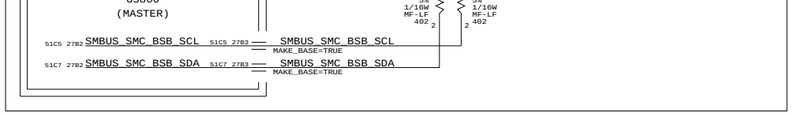
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M57 SMBUS CONNECTIONS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	27	87

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot

MEMVREF_OUT

C2801 2.2uF 20% 6.3V CERM 603

C2800 0.1uF 20% 10V CERM 402

PP1V8_S3

NC

CRITICAL

J2800
F-RT-SM-M9

DDR2-SODIMM-DUAL

		VREF	1A	VSS0	2A		
		VSS1	3A	DQ4	4A	MEM_A_DQ<8>	15C7
MEM_A_DQ<14>	15C7	DQ0	5A	DQ5	6A	MEM_A_DQ<12>	15C7
MEM_A_DQ<13>	15C7	DQ1	7A	VSS2	8A		
		VSS4	9A	DM0	10A	MEM_A_DM<1>	15D5
MEM_A_DQS_N<1>	15C5	DQS0*	11A	VSS5	12A		
MEM_A_DQS_P<1>	15C5	DQS0	13A	DQ6	14A	MEM_A_DQ<15>	15C7
		VSS6	15A	DQ7	16A	MEM_A_DQ<9>	15C7
MEM_A_DQ<10>	15C7	DQ2	17A	VSS7	18A		
MEM_A_DQ<11>	15C7	DQ3	19A	DQ12	20A	MEM_A_DQ<2>	15D7
		VSS8	21A	DQ13	22A	MEM_A_DQ<3>	15D7
MEM_A_DQ<5>	15D7	DQ8	23A	VSS9	24A		
MEM_A_DQ<4>	15D7	DQ9	25A	DM1	26A	MEM_A_DM<0>	15D5
		VSS10	27A	VSS11	28A		
MEM_A_DQS_N<0>	15C5	DQS1*	29A	CK0	30A	MEM_CLK_P<0>	14D4
MEM_A_DQS_P<0>	15C5	DQS1	31A	CK0*	32A	MEM_CLK_N<0>	14D4
		VSS12	33A	VSS13	34A		
MEM_A_DQ<6>	15D7	DQ10	35A	DQ14	36A	MEM_A_DQ<1>	15D7
MEM_A_DQ<7>	15D7	DQ11	37A	DQ15	38A	MEM_A_DQ<0>	15D7
		VSS14	39A	VSS15	40A		
				KEY			
		VSS16	41A	VSS17	42A		
MEM_A_DQ<19>	15C7	DQ16	43A	DQ20	44A	MEM_A_DQ<23>	15C7
MEM_A_DQ<18>	15C7	DQ17	45A	DQ21	46A	MEM_A_DQ<22>	15C7
		VSS18	47A	VSS19	48A		
MEM_A_DQS_N<2>	15C5	DQS2*	49A	NC0	50A	PM_EXTTS_L	14B7 29C3 51B7 52D3 52D5
MEM_A_DQS_P<2>	15C5	DQS2	51A	DM2	52A	MEM_A_DM<2>	15D5
		VSS21	53A	VSS22	54A		
MEM_A_DQ<20>	15C7	DQ18	55A	DQ22	56A	MEM_A_DQ<21>	15C7
MEM_A_DQ<16>	15C7	DQ19	57A	DQ23	58A	MEM_A_DQ<17>	15C7
		VSS23	59A	VSS24	60A		
MEM_A_DQ<28>	15C7	DQ24	61A	DQ28	62A	MEM_A_DQ<29>	15C7
MEM_A_DQ<25>	15C7	DQ25	63A	DQ29	64A	MEM_A_DQ<24>	15C7
		VSS25	65A	VSS26	66A		
MEM_A_DM<3>	15C5	DM3	67A	DQS3*	68A	MEM_A_DQS_N<3>	15C5
NC		NC1	69A	DQS3	70A	MEM_A_DQS_P<3>	15C5
		VSS27	71A	VSS28	72A		
MEM_A_DQ<27>	15C7	DQ26	73A	DQ30	74A	MEM_A_DQ<26>	15C7
MEM_A_DQ<30>	15C7	DQ27	75A	DQ31	76A	MEM_A_DQ<31>	15C7
		VSS29	77A	VSS30	78A		
MEM_CKE<0>	30D6 14C4	CKE0	79A	NC/CKE1	80A	MEM_CKE<1>	14C4 30D6
		VDD0	81A	VDD1	82A		
NC		NC2	83A	NC/A15	84A	NC_MEM_A_A<15>	6D7
MEM_A_BS<2>	30B6 15D5	BA2	85A	NC/A14	86A	NC_MEM_A_A<14>	6D7
		VDD2	87A	VDD3	88A		
MEM_A_A<12>	30C6 15B5	A12	89A	A11	90A	MEM_A_A<11>	15B5 30C6
MEM_A_A<9>	30C6 15B5	A9	91A	A7	92A	MEM_A_A<7>	15B5 30C6
MEM_A_A<8>	30C6 15B5	A8	93A	A6	94A	MEM_A_A<6>	15B5 30C6
		VDD4	95A	VDD5	96A		
MEM_A_A<5>	30C6 15B5	A5	97A	A4	98A	MEM_A_A<4>	15B5 30C6
MEM_A_A<3>	30C6 15B5	A3	99A	A2	100A	MEM_A_A<2>	15C5 30C6
MEM_A_A<1>	30C6 15C5	A1	101A	A0	102A	MEM_A_A<0>	15C5 30C6
		VDD6	103A	VDD7	104A		
MEM_A_A<10>	30C6 15B5	A10/AP	105A	BA1	106A	MEM_A_BS<1>	15D5 30B6
MEM_A_BS<0>	30B6 15D5	BA0	107A	RAS*	108A	MEM_A_RAS_L	15B5 30B6
MEM_A_WE_L	30B6 15B5	WE*	109A	S0*	110A	MEM_CS_L<0>	14C4 30D6
		VDD8	111A	VDD9	112A		
MEM_A_CAS_L	30B6 15D5	CAS*	113A	ODT0	114A	MEM_ODT<0>	14C4 30C6
MEM_CS_L<1>	30D6 14C4	NC/S1*	115A	NC/A13	116A	MEM_A_A<13>	15B5 30C6
		VDD10	117A	VDD11	118A		
MEM_ODT<1>	30C6 14C4	NC/ODT1	119A	NC3	120A	NC	
		VSS31	121A	VSS32	122A		
MEM_A_DQ<35>	15B7	DQ32	123A	DQ36	124A	MEM_A_DQ<38>	15B7
MEM_A_DQ<39>	15B7	DQ33	125A	DQ37	126A	MEM_A_DQ<34>	15B7
		VSS33	127A	VSS34	128A		
MEM_A_DQS_N<4>	15C5	DQS4*	129A	DM4	130A	MEM_A_DM<4>	15C5
MEM_A_DQS_P<4>	15C5	DQS4	131A	VSS35	132A		
		VSS36	133A	DQ38	134A	MEM_A_DQ<32>	15C7
MEM_A_DQ<37>	15B7	DQ34	135A	DQ39	136A	MEM_A_DQ<36>	15B7
MEM_A_DQ<33>	15C7	DQ35	137A	VSS37	138A		
		VSS38	139A	DQ44	140A	MEM_A_DQ<57>	15B7
MEM_A_DQ<60>	15A7	DQ40	141A	DQ45	142A	MEM_A_DQ<63>	15A7
MEM_A_DQ<59>	15B7	DQ41	143A	VSS39	144A		
		VSS40	145A	DQS5*	146A	MEM_A_DQS_N<7>	15C5
MEM_A_DM<7>	15C5	DM5	147A	DQS5	148A	MEM_A_DQS_P<7>	15C5
		VSS41	149A	VSS42	150A		
MEM_A_DQ<58>	15B7	DQ42	151A	DQ46	152A	MEM_A_DQ<56>	15B7
MEM_A_DQ<61>	15A7	DQ43	153A	DQ47	154A	MEM_A_DQ<62>	15A7
		VSS43	155A	VSS44	156A		
MEM_A_DQ<43>	15B7	DQ48	157A	DQ52	158A	MEM_A_DQ<40>	15B7
MEM_A_DQ<45>	15B7	DQ49	159A	DQ53	160A	MEM_A_DQ<42>	15B7
		VSS45	161A	VSS46	162A		
NC		NC_TEST	163A	CK1	164A	MEM_CLK_P<1>	14D4
		VSS47	165A	CK1*	166A	MEM_CLK_N<1>	14D4
MEM_A_DQS_N<5>	15C5	DQS6*	167A	VSS48	168A		
MEM_A_DQS_P<5>	15C5	DQS6	169A	DM6	170A	MEM_A_DM<5>	15C5
		VSS49	171A	VSS50	172A		
MEM_A_DQ<41>	15B7	DQ50	173A	DQ54	174A	MEM_A_DQ<47>	15B7
MEM_A_DQ<46>	15B7	DQ51	175A	DQ55	176A	MEM_A_DQ<44>	15B7
		VSS51	177A	VSS52	178A		
MEM_A_DQ<51>	15B7	DQ56	179A	DQ60	180A	MEM_A_DQ<54>	15B7
MEM_A_DQ<50>	15B7	DQ57	181A	DQ61	182A	MEM_A_DQ<55>	15B7
		VSS53	183A	VSS54	184A		
MEM_A_DM<6>	15C5	DM7	185A	DQS7*	186A	MEM_A_DQS_N<6>	15C5
		VSS55	187A	DQS7	188A	MEM_A_DQS_P<6>	15C5
MEM_A_DQ<53>	15B7	DQ58	189A	VSS56	190A		
MEM_A_DQ<48>	15B7	DQ59	191A	DQ62	192A	MEM_A_DQ<52>	15B7
		VSS57	193A	DQ63	194A	MEM_A_DQ<49>	15B7
PP3V3_S0				VSS58	196A		
SMBUS_SB_SDA	46B6 33B6 29A6 27D8 27D7 27D6 27C6 27B6 23D5 5B1 81C3 48B3	SDA	195A				
SMBUS_SB_SCL	46B6 33B6 29A6 27D8 27D7 27D6 27C6 27B6 23D5 5B1 81C3 48B3	SCL	197A	SA0	198A		
		VDDSPD	199A	SA1	200A	ADDR=0x0A0(WR)/0xA1(RD)	

203 201 NC

202 204 NC

516S0471

PP1V8_S3

C2808 10UF 20% 6.3V XSR 603

C2809 10UF 20% 6.3V XSR 603

C2810 1UF 10% 6.3V CERM 402

C2811 1UF 10% 6.3V CERM 402

C2812 1UF 10% 6.3V CERM 402

C2813 1UF 10% 6.3V CERM 402

C2814 1UF 10% 6.3V CERM 402

C2815 1UF 10% 6.3V CERM 402

C2816 1UF 10% 6.3V CERM 402

C2817 1UF 10% 6.3V CERM 402

C2818 1UF 10% 6.3V CERM 402

C2819 1UF 10% 6.3V CERM 402

C2820 1UF 10% 6.3V CERM 402

C2821 1UF 10% 6.3V CERM 402

DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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SCALE: NONE	SHT 28 OF 87	

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Factory" (thru-hole) slot

MEMVREF_OUT

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

PP1V8_S3

DDR2-SODIMM-DUAL

CRITICAL
J2900
F-RT-TH1

		VREF	1B	VSS0	2B		
		VSS1	3B	DQ4	4B	MEM_B_DQ<9>	15C4
15C4	MEM_B_DQ<15>	DQ0	5B	DQ5	6B	MEM_B_DQ<11>	15C4
15C4	MEM_B_DQ<14>	DQ1	7B	VSS2	8B		
		VSS4	9B	DM0	10B	MEM_B_DM<1>	15D2
15C2	MEM_B_DQS_N<1>	DQS0*	11B	VSS5	12B		
15C2	MEM_B_DQS_P<1>	DQS0	13B	DQ6	14B	MEM_B_DQ<12>	15C4
		VSS6	15B	DQ7	16B	MEM_B_DQ<8>	15C4
15C4	MEM_B_DQ<10>	DQ2	17B	VSS7	18B		
15C4	MEM_B_DQ<13>	DQ3	19B	DQ12	20B	MEM_B_DQ<3>	15D4
		VSS8	21B	DQ13	22B	MEM_B_DQ<6>	15D4
15D4	MEM_B_DQ<7>	DQ8	23B	VSS9	24B		
15D4	MEM_B_DQ<2>	DQ9	25B	DM1	26B	MEM_B_DM<0>	15D2
		VSS10	27B	VSS11	28B		
15C2	MEM_B_DQS_N<0>	DQS1*	29B	CK0	30B	MEM_CLK_P<3>	14D4
15C2	MEM_B_DQS_P<0>	DQS1	31B	CK0*	32B	MEM_CLK_N<3>	14D4
		VSS12	33B	VSS13	34B		
15D4	MEM_B_DQ<1>	DQ10	35B	DQ14	36B	MEM_B_DQ<0>	15D4
15D4	MEM_B_DQ<4>	DQ11	37B	DQ15	38B	MEM_B_DQ<5>	15D4
		VSS14	39B	VSS15	40B		
		KEY					
		VSS16	41B	VSS17	42B		
15C4	MEM_B_DQ<21>	DQ16	43B	DQ20	44B	MEM_B_DQ<22>	15C4
15C4	MEM_B_DQ<19>	DQ17	45B	DQ21	46B	MEM_B_DQ<18>	15C4
		VSS18	47B	VSS19	48B		
15C2	MEM_B_DQS_N<2>	DQS2*	49B	NC0	50B	PM_EXTTS_L	14B7 28C3 51B7 52D3 52D5
15C2	MEM_B_DQS_P<2>	DQS2	51B	DM2	52B	MEM_B_DM<2>	15D2
		VSS21	53B	VSS22	54B		
15C4	MEM_B_DQ<20>	DQ18	55B	DQ22	56B	MEM_B_DQ<17>	15C4
15C4	MEM_B_DQ<23>	DQ19	57B	DQ23	58B	MEM_B_DQ<16>	15C4
		VSS23	59B	VSS24	60B		
15C4	MEM_B_DQ<29>	DQ24	61B	DQ28	62B	MEM_B_DQ<26>	15C4
15C4	MEM_B_DQ<24>	DQ25	63B	DQ29	64B	MEM_B_DQ<28>	15C4
		VSS25	65B	VSS26	66B		
15C2	MEM_B_DM<3>	DM3	67B	DQS3*	68B	MEM_B_DQS_N<3>	15C2
	NC	NC1	69B	DQS3	70B	MEM_B_DQS_P<3>	15C2
		VSS27	71B	VSS28	72B		
15C4	MEM_B_DQ<27>	DQ26	73B	DQ30	74B	MEM_B_DQ<31>	15C4
15C4	MEM_B_DQ<25>	DQ27	75B	DQ31	76B	MEM_B_DQ<30>	15C4
		VSS29	77B	VSS30	78B		
30D6 14C4	MEM_CKE<2>	CKE0	79B	NC/CKE1	80B	MEM_CKE<3>	14C4 30D6
		VDD0	81B	VDD1	82B		
	NC	NC2	83B	NC/A15	84B	NC_MEM_B_A<15>	6D7
30A6 15D2	MEM_B_BS<2>	BA2	85B	NC/A14	86B	NC_MEM_B_A<14>	6D7
		VDD2	87B	VDD3	88B		
30B6 15B2	MEM_B_A<12>	A12	89B	A11	90B	MEM_B_A<11>	15B2 30B6
30B6 15B2	MEM_B_A<9>	A9	91B	A7	92B	MEM_B_A<7>	15B2 30B6
30B6 15B2	MEM_B_A<8>	A8	93B	A6	94B	MEM_B_A<6>	15B2 30B6
		VDD4	95B	VDD5	96B		
30B6 15B2	MEM_B_A<5>	A5	97B	A4	98B	MEM_B_A<4>	15B2 30B6
30B6 15B2	MEM_B_A<3>	A3	99B	A2	100B	MEM_B_A<2>	15C2 30B6
30B6 15C2	MEM_B_A<1>	A1	101B	A0	102B	MEM_B_A<0>	15C2 30B6
		VDD6	103B	VDD7	104B		
30B6 15B2	MEM_B_A<10>	A10/AP	105B	BA1	106B	MEM_B_BS<1>	15D2 30A6
30A6 15D2	MEM_B_BS<0>	BA0	107B	RAS*	108B	MEM_B_RAS_L	15B2 30A6
30A6 15B2	MEM_B_WE_L	WE*	109B	S0*	110B	MEM_CS_L<2>	14C4 30D6
		VDD8	111B	VDD9	112B		
30A6 15D2	MEM_B_CAS_L	CAS*	113B	ODT0	114B	MEM_ODT<2>	14C4 30C6
30D6 14C4	MEM_CS_L<3>	NC/S1*	115B	NC/A13	116B	MEM_B_A<13>	15B2 30B6
		VDD10	117B	VDD11	118B		
30C6 14C4	MEM_ODT<3>	NC/ODT1	119B	NC3	120B	NC	
		VSS31	121B	VSS32	122B		
15B4	MEM_B_DQ<36>	DQ32	123B	DQ36	124B	MEM_B_DQ<32>	15C4
15C4	MEM_B_DQ<33>	DQ33	125B	DQ37	126B	MEM_B_DQ<37>	15B4
		VSS33	127B	VSS34	128B		
15C2	MEM_B_DQS_N<4>	DQS4*	129B	DM4	130B	MEM_B_DM<4>	15C2
15C2	MEM_B_DQS_P<4>	DQS4	131B	VSS35	132B		
		VSS36	133B	DQ38	134B	MEM_B_DQ<38>	15B4
15B4	MEM_B_DQ<34>	DQ34	135B	DQ39	136B	MEM_B_DQ<39>	15B4
15B4	MEM_B_DQ<35>	DQ35	137B	VSS37	138B		
		VSS38	139B	DQ44	140B	MEM_B_DQ<44>	15B4
15B4	MEM_B_DQ<40>	DQ40	141B	DQ45	142B	MEM_B_DQ<45>	15B4
15B4	MEM_B_DQ<41>	DQ41	143B	VSS39	144B		
		VSS40	145B	DQS5*	146B	MEM_B_DQS_N<5>	15C2
15C2	MEM_B_DM<5>	DM5	147B	DQS5	148B	MEM_B_DQS_P<5>	15C2
		VSS41	149B	VSS42	150B		
15B4	MEM_B_DQ<42>	DQ42	151B	DQ46	152B	MEM_B_DQ<46>	15B4
15B4	MEM_B_DQ<43>	DQ43	153B	DQ47	154B	MEM_B_DQ<47>	15B4
		VSS43	155B	VSS44	156B		
15A4	MEM_B_DQ<62>	DQ48	157B	DQ52	158B	MEM_B_DQ<58>	15B4
15B4	MEM_B_DQ<59>	DQ49	159B	DQ53	160B	MEM_B_DQ<63>	15A4
		VSS45	161B	VSS46	162B		
	NC	NC_TEST	163B	CK1	164B	MEM_CLK_P<2>	14D4
		VSS47	165B	CK1*	166B	MEM_CLK_N<2>	14D4
15C2	MEM_B_DQS_N<7>	DQS6*	167B	VSS48	168B		
15C2	MEM_B_DQS_P<7>	DQS6	169B	DM6	170B	MEM_B_DM<7>	15C2
		VSS49	171B	VSS50	172B		
15A4	MEM_B_DQ<60>	DQ50	173B	DQ54	174B	MEM_B_DQ<56>	15B4
15A4	MEM_B_DQ<61>	DQ51	175B	DQ55	176B	MEM_B_DQ<57>	15B4
		VSS51	177B	VSS52	178B		
15B4	MEM_B_DQ<54>	DQ56	179B	DQ60	180B	MEM_B_DQ<55>	15B4
15B4	MEM_B_DQ<51>	DQ57	181B	DQ61	182B	MEM_B_DQ<50>	15B4
		VSS53	183B	VSS54	184B		
15C2	MEM_B_DM<6>	DM7	185B	DQS7*	186B	MEM_B_DQS_N<6>	15C2
		VSS55	187B	DQS7	188B	MEM_B_DQS_P<6>	15C2
15B4	MEM_B_DQ<52>	DQ58	189B	VSS56	190B		
15B4	MEM_B_DQ<49>	DQ59	191B	DQ62	192B	MEM_B_DQ<53>	15B4
		VSS57	193B	DQ63	194B	MEM_B_DQ<48>	15B4
	SMBUS_SB_SDA	SDA	195B	VSS58	196B	Resistor prevents pwr-gnd short	
	SMBUS_SB_SCL	SCL	197B	SA0	198B		
		VDDSPD	199B	SA1	200B	SODIMM_A_SA1	

PP3V3_S0

516-0140

201 NC

202 NC

ADDR=0xA4(WR)/0xA5(RD)

PP3V3_S0 — R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2908	10UF 20% 5.3V XSR 603	
C2909	10UF 20% 5.3V XSR 603	
C2910	1UF 10% 6.3V CERM 402	
C2911	0.1uF 20% 10V CERM 402	
C2912	1UF 10% 6.3V CERM 402	
C2913	1UF 10% 6.3V CERM 402	
C2914	1UF 10% 6.3V CERM 402	
C2915	1UF 10% 6.3V CERM 402	
C2916	1UF 10% 6.3V CERM 402	
C2917	0.1uF 20% 10V CERM 402	
C2918	0.1uF 20% 10V CERM 402	
C2919	0.1uF 20% 10V CERM 402	
C2920	0.1uF 20% 10V CERM 402	
C2921	0.1uF 20% 10V CERM 402	

DDR2 SO-DIMM Connector B

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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D	051-7164	06004

SCALE: NONE SHT 29 OF 87

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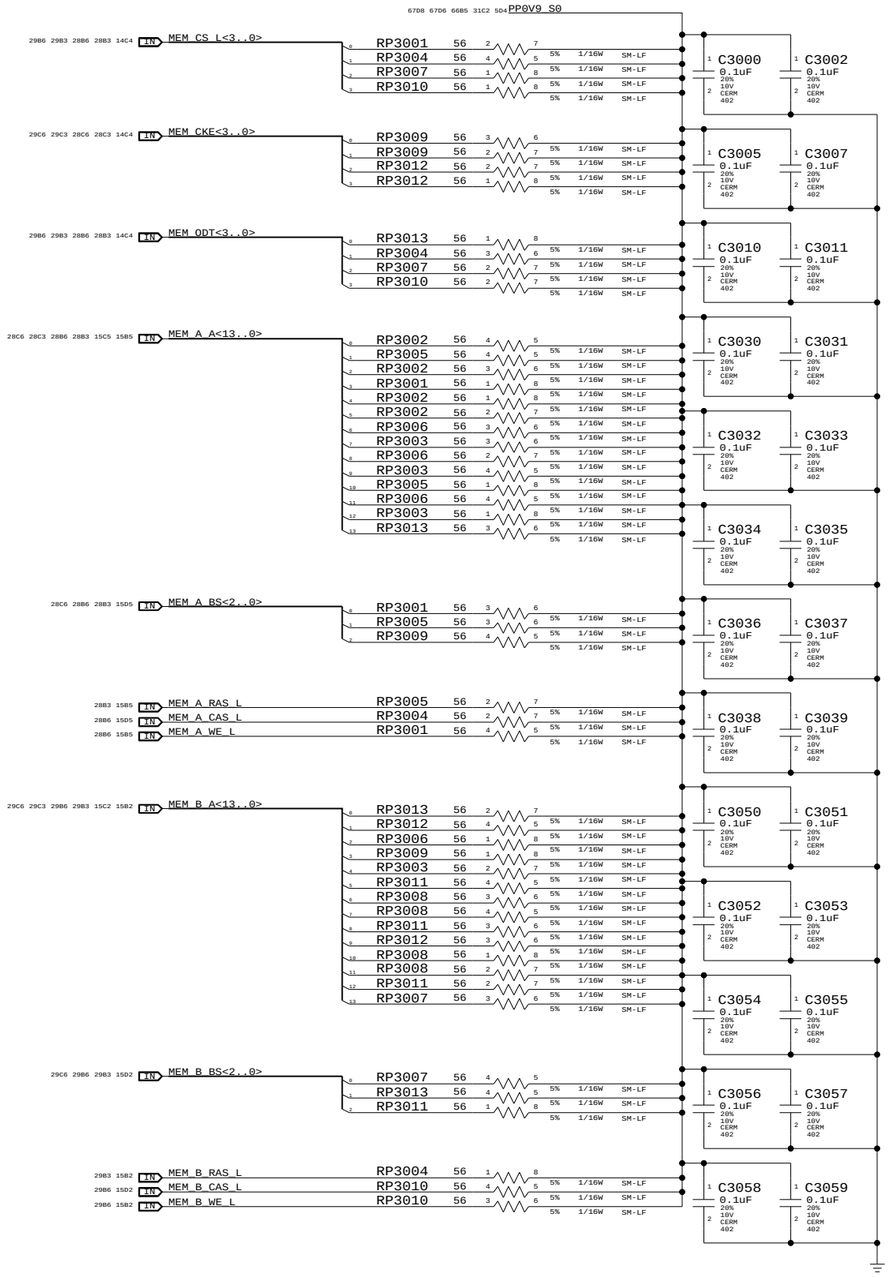
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	30	87

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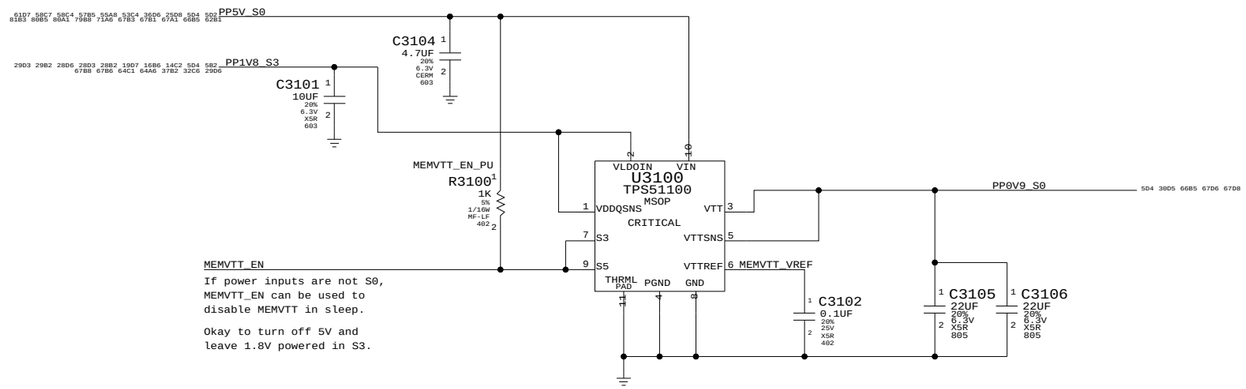
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 31 OF 87

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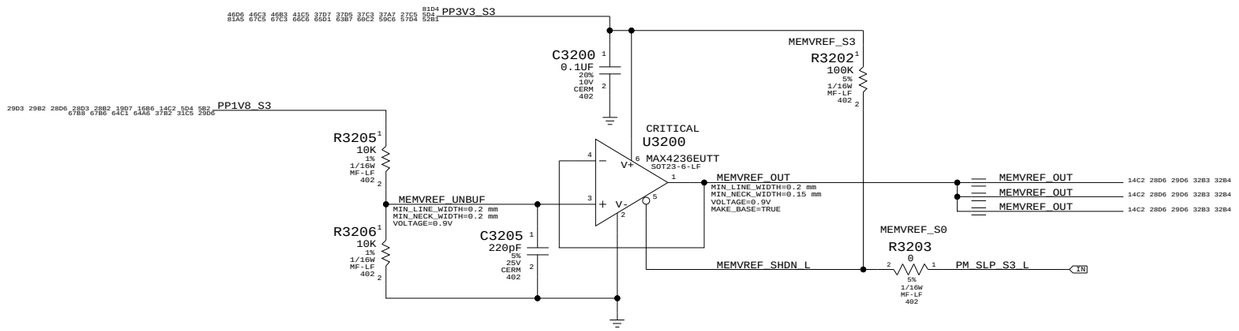

DDR2 VRef

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 32 OF 87

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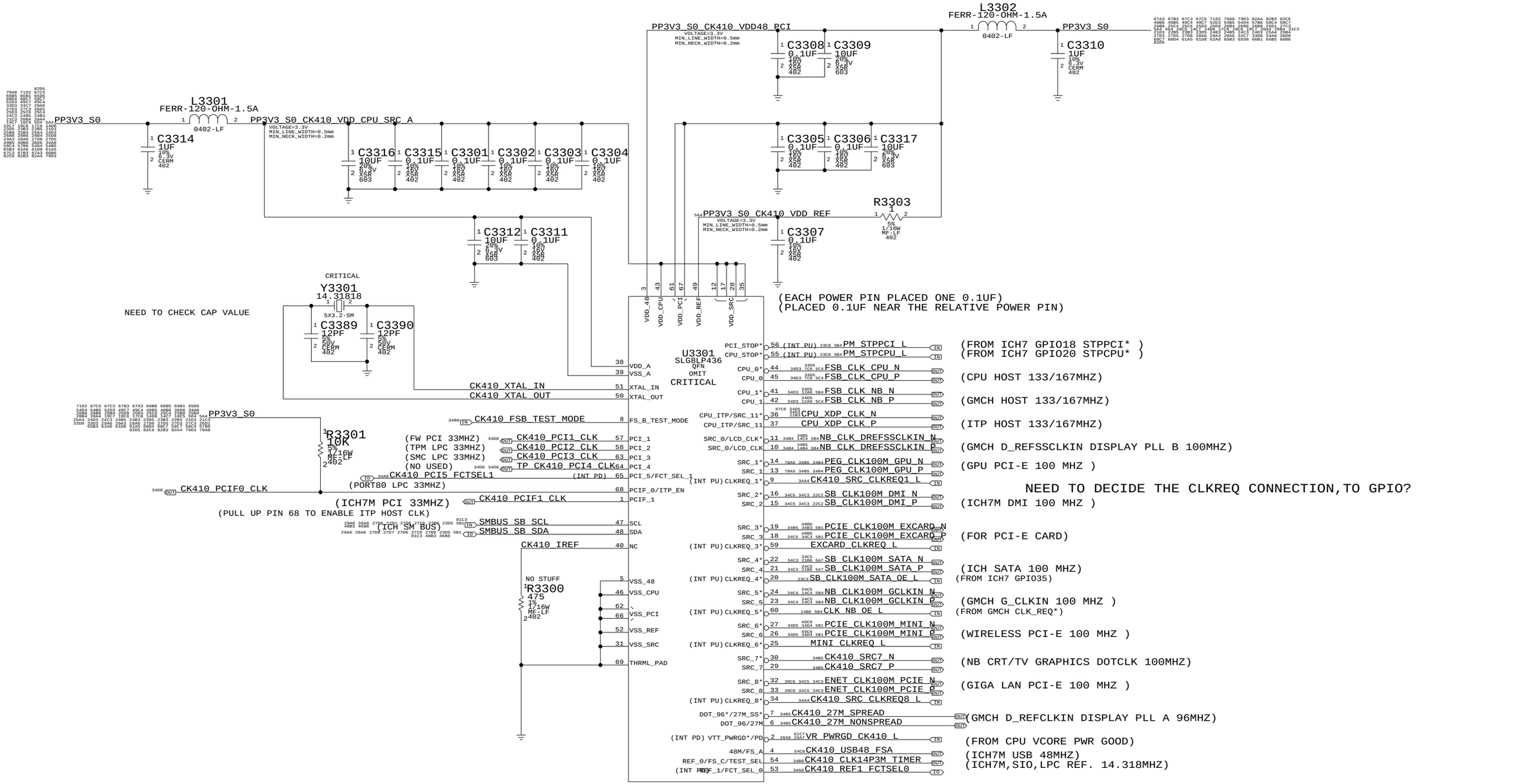

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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D	051-7164	06004
SCALE: NONE	SHT 33 OF 87	

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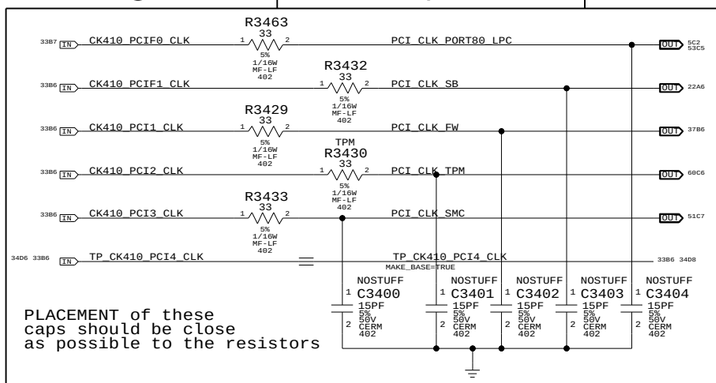

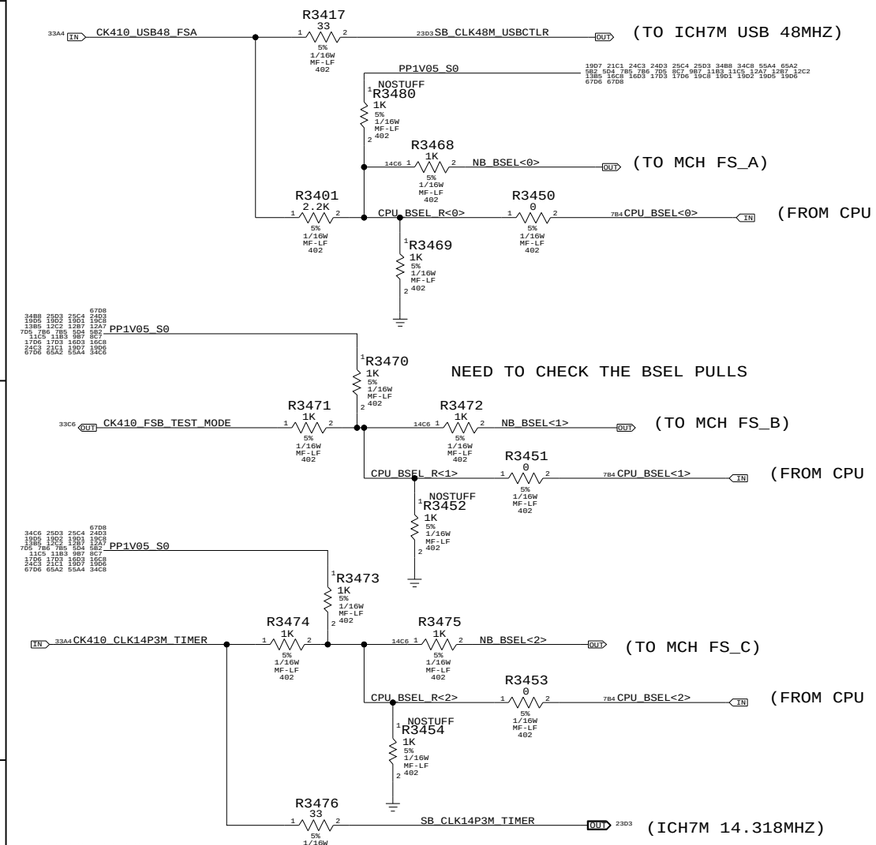

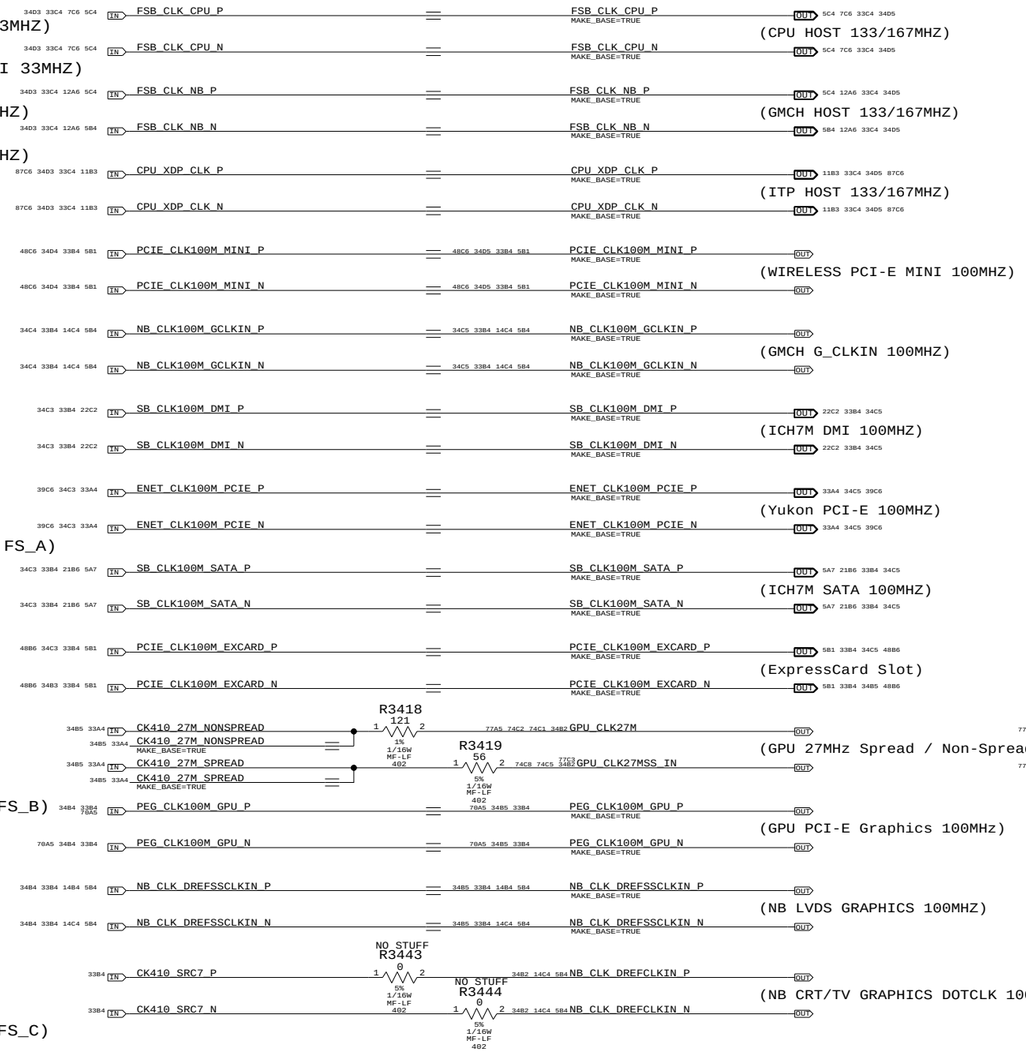

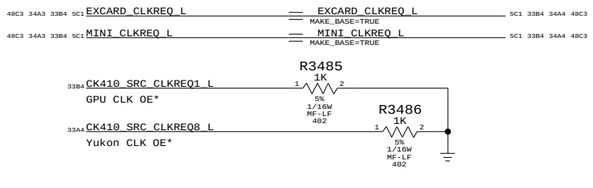

NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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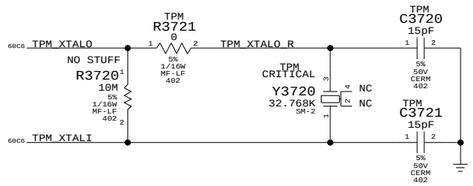
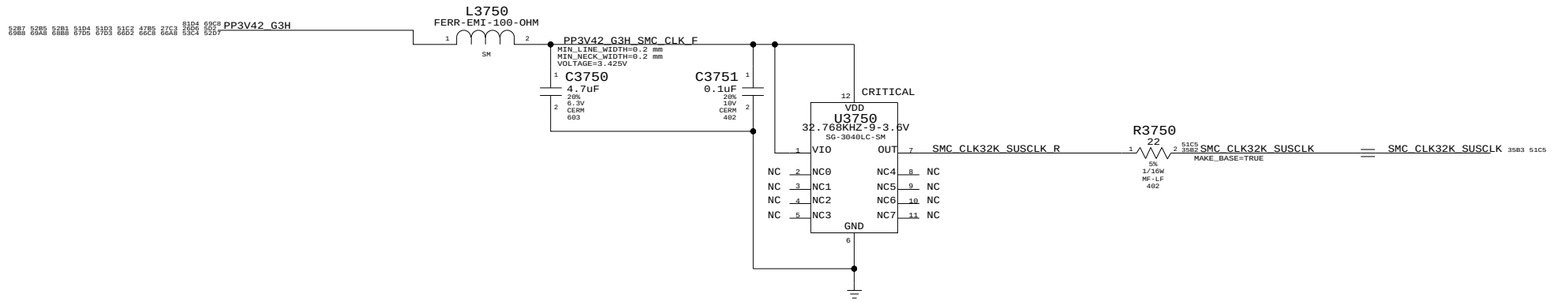
TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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D	051-7164	06004

SCALE	SHT	OF
NONE	35	87

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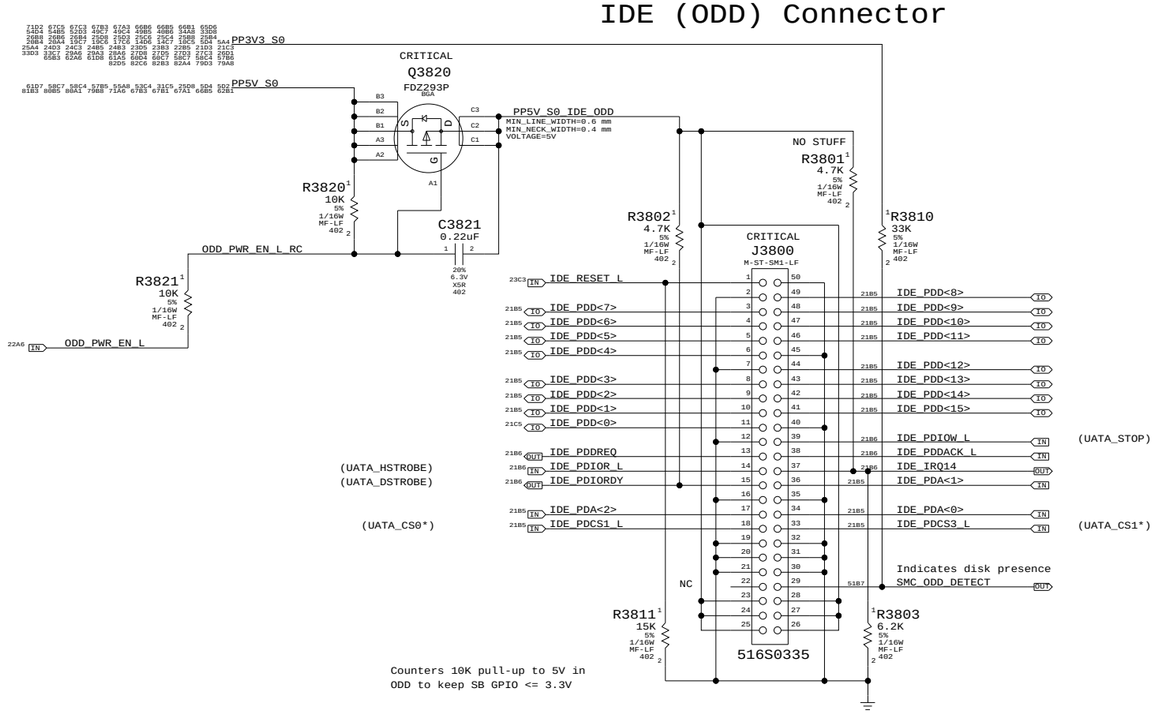
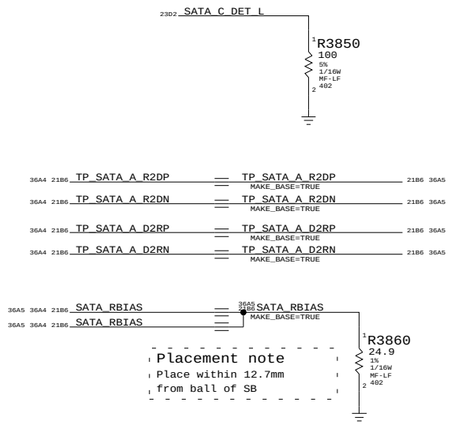
IDE (ODD) Connector





PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	36	87

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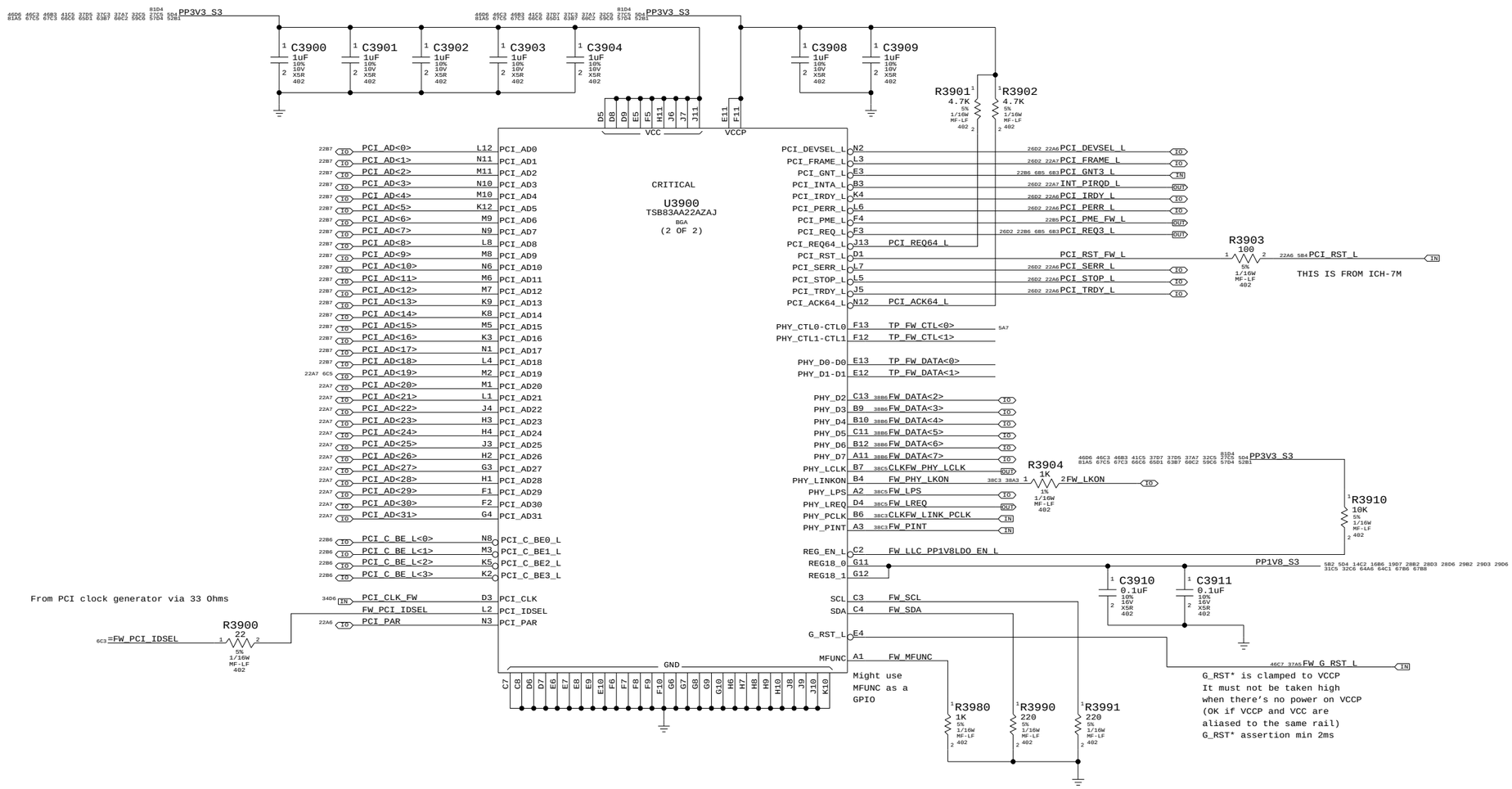

FireWire Link (TSB83AA22)

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SCALE	SHT	OF
NONE	37	87

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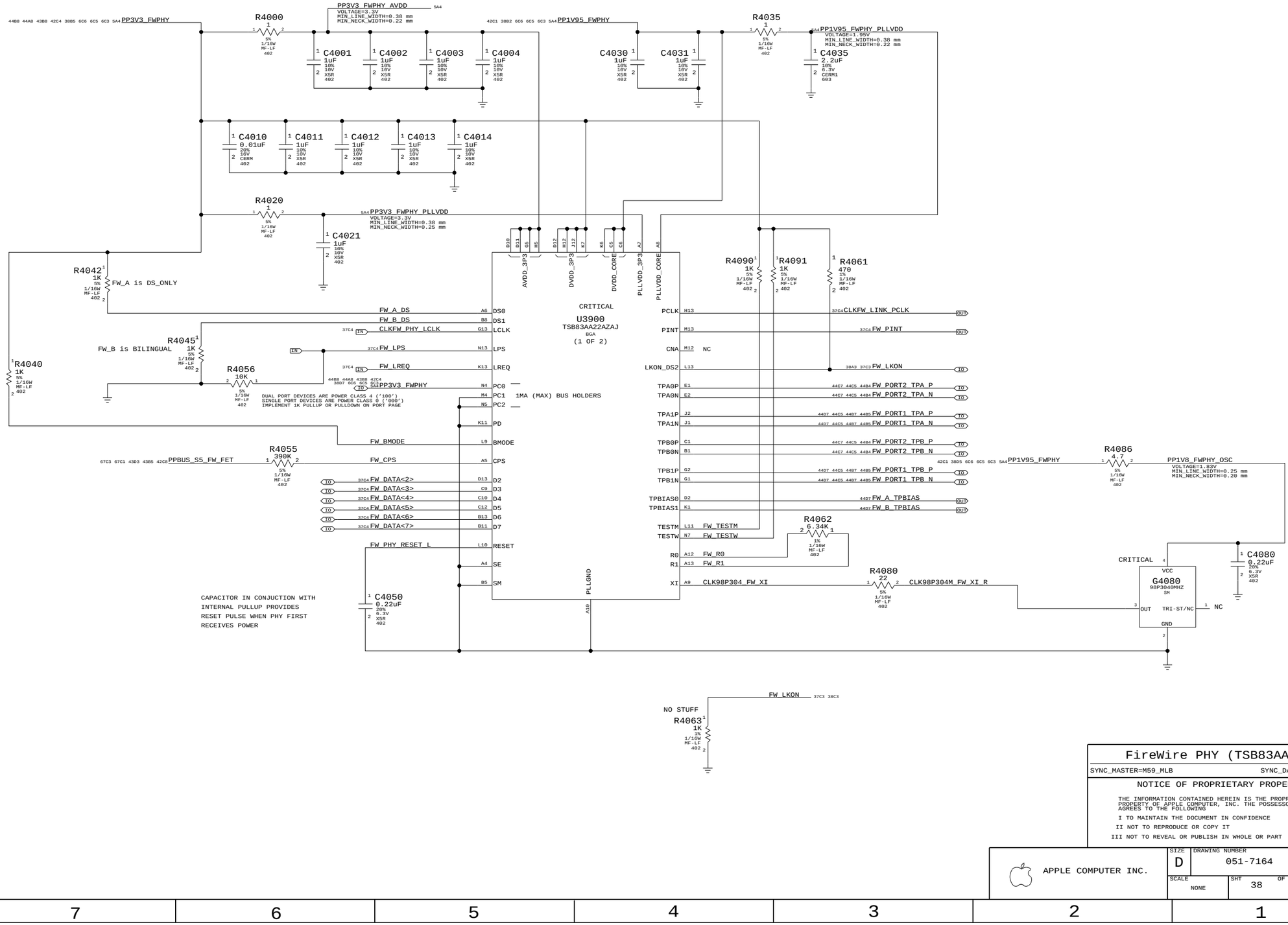

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PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

PLACE C4107 NEAR U4101 AVDD

L4100
FERR-120-OHM-1.5A
0402-LF
PP2V5_S3

PP3V3_S3AC
PP1V2_S3
PP3V3_S3AC

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF X5R 10% 16V 402
C4113 0.1UF X5R 16V 10% 402

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

OMIT
CRITICAL
U4101
88E8053
QFN

ENET_LOM_DIS_L
PM_SLP_S3_L
NC_ENET_CTRL25
NC_ENET_CTRL12
ENET_RSET

ANALOG
PCI EXPRESS
LED
TEST
TWSI
SPI
MAIN CLK
MEDIA

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

R4102 4.87K 1% 1/16W MF-LF 402

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053
INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO
Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD

ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

Setting attribute VOLTAGE
to arbitrary value
to help constraint manager
find correct topolgy

PLACE RESISTORS CLOSE TO U4101

Q4100 2N7002 SOT23-LF
ENET_LOWPWR_EN
R4132 100K 5% 1/16W MF-LF 402
R4101 4.7K 5% 1/16W MF-LF 402
R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8
VCC
E2
NC1
NC0
WC*
VSS
SDA
SCL

R4122 10K 5% 1/16W MF-LF 402
R4123 10K 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M59_MLB
SYNC_DATE=09/15/2006

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40D3
	ENETCONN	ENET_100D	ENETCONN_N<0> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<3> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<3> 40B3

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board

39D5 5A4 IN PP2V5_S3_ENET_AVDD

Place one cap at each pin of transformer

C4200 1uF 10% 6.3V CERM 402
C4201 1uF 10% 6.3V CERM 402
C4202 1uF 10% 6.3V CERM 402
C4203 1uF 10% 6.3V CERM 402

1000BT-824-00275
T4200 XFR-SM CRITICAL
SYM_VER2

39C3 IO ENET_MDI_P<0>
40B7 39C3 IO ENET_MDI_N<0>
39C3 IO ENET_MDI_P<1>
40A7 39C3 IO ENET_MDI_N<1>

1000BT-824-00275
T4201 XFR-SM CRITICAL
SYM_VER2

39C3 IO ENET_MDI_P<2>
39C3 IO ENET_MDI_N<2>
39C3 IO ENET_MDI_P<3>
39C3 IO ENET_MDI_N<3>

CRITICAL
J4200
JM36113-P2054-7F
F-RT-TH-RJ45

514-0277
Short shielded RJ-45

NO STUFF
R4210 0 5% 1/16W MF-LF 402
Place close to connector

R4200 75 5% 1/16W MF-LF 402
R4201 75 5% 1/16W MF-LF 402
R4202 75 5% 1/16W MF-LF 402
R4203 75 5% 1/16W MF-LF 402

ENET_CTAP_COMMON
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C4204 100pF 10% 3KV CERM 1808

GND_CHASSIS_ENET OUT

LAN ENERGY DETECT

PP3V3_S0

R4227 470K 1% 1/16W MF-LF 402
R4223 3.3K 5% 1/16W MF-LF 402
R4228 392K 1% 1/16W MF-LF 402
R4224 100K 1% 1/16W MF-LF 402
C4223 0.1uF 10% 16V X5R 402

40C4 39C3 ENET_MDI_N<0>
C4220 68PF 5% 50V CERM 402-1
ED_MDIN0_C VOLTAGE=1.234V
R4220 2.4K 5% 1/16W MF-LF 402

40C4 39C3 ENET_MDI_N<1>
C4221 68PF 5% 50V CERM 402-1
ED_MDIN1_C VOLTAGE=1.234V
R4221 2.4K 5% 1/16W MF-LF 402

EDET_MDIN_AMP
ED_MDIN_R
Q4220 MMDT3904XF SOT-363-LF
Q4220 MMDT3904XF SOT-363-LF

NO STUFF
C4222 100pF 5% 50V CERM 402
R4225 51.1K 1% 1/16W MF-LF 402

EDET_ACT
EDET_REF
U4200 LMC7211 SM-LF
LAN_ENERGY_DET 23C3
R4226 10K 5% 1/16W MF-LF 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

PLACE C4220 & C4221
NEAR ENET_MDI_N<0/1>

Ethernet Connector

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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SCALE: NONE	SHT 40 OF 87	

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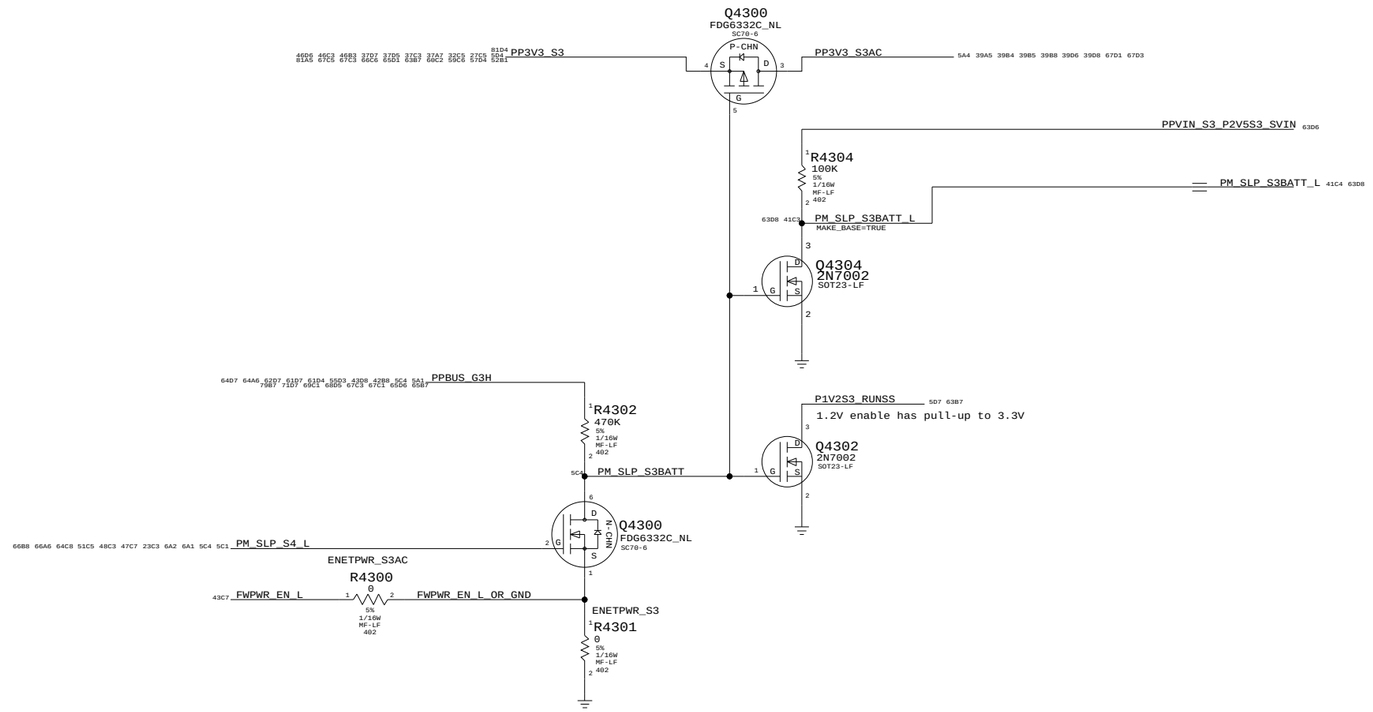
Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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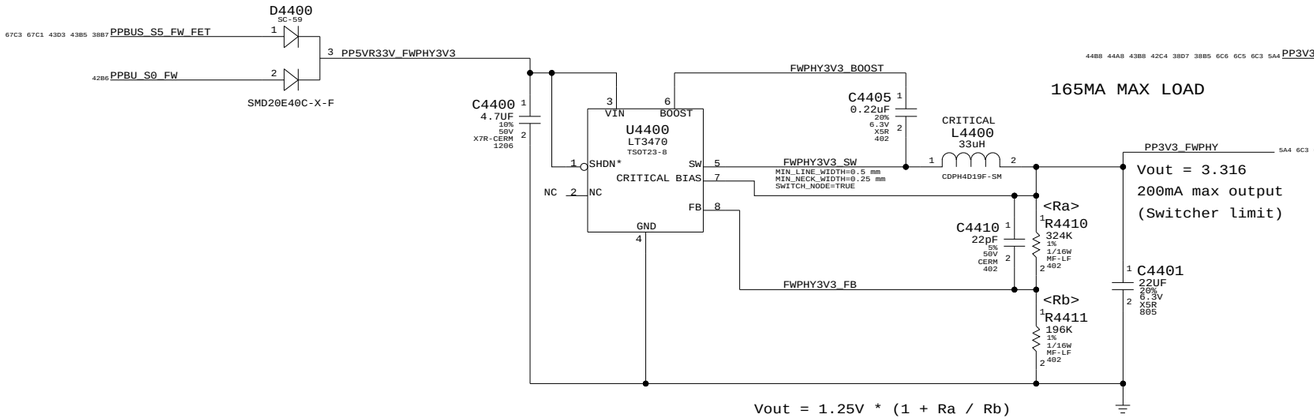
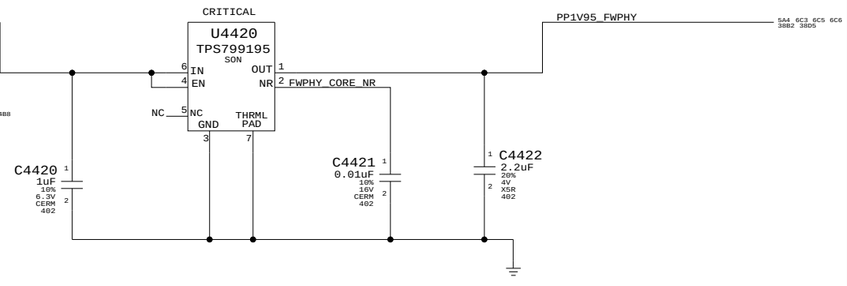
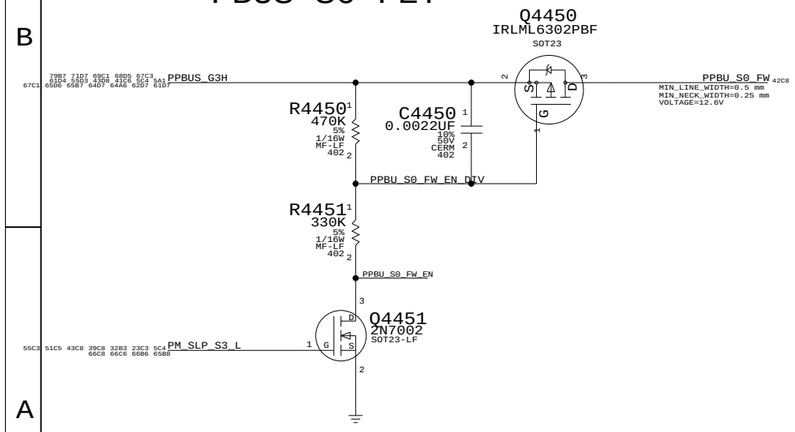
3.3V Supply for FWPHY



1.95V Supply for FW PHY



PBUS S0 FET



Vout = 1.25V * (1 + Ra / Rb)

FW PHY Power Supply

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D	051-7164	06004

SCALE	SHT	OF
NONE	42	87

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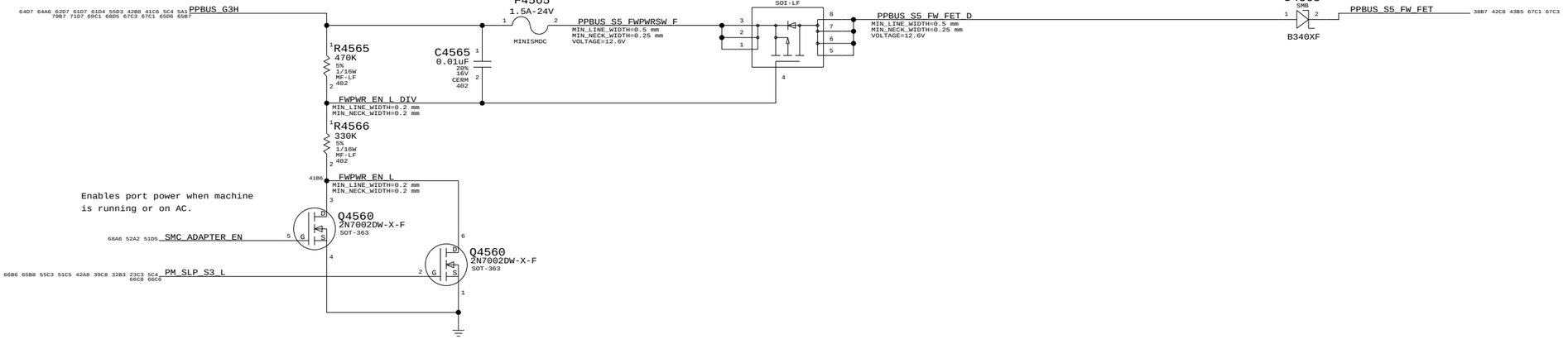
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

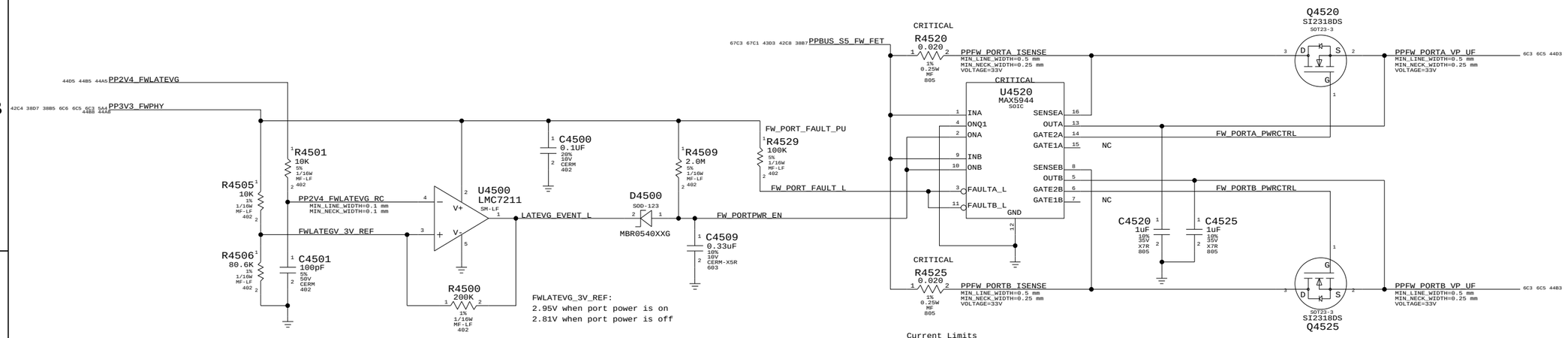
BOM options provided by this page:
(NONE)

Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	38B3 44B5 44B7 44C5
	FW	FW_110D	FW_PORT1_TPA_N	38B3 44B5 44B7 44C5
BY	FW	FW_110D	FW_PORT1_TPB_P	38B3 44B5 44B7 44C5
	FW	FW_110D	FW_PORT1_TPB_N	38B3 44B5 44B7 44C5
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPA_FL_N	44B2
	FW	FW_110D	FW_PORT2_TPB_FL_P	44B2
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_N	44B2

AREF needs to be isolated from
all local grounds per 1394b spec

When a bilingual device is
connected to a beta-only device,
there is no DC path between them
(to avoid ground offset issue)

BREF should be hard-connected to
logic ground for speed signaling
and connection detection currents
per 1394b V1.33

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

Late-VG Protection Power

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

ESD and late-VG rail for snap-back diodes (Common to all ports)

"Snapback" & "Late VG" Protection

Cable Power

Note:Trace PPFW_PORT1_VP should handle up to 5A

PORT 1
BILINGUAL

"Snapback" & "Late VG" Protection

Cable Power

PORT 2
1394A

FireWire Ports	
SYNC_MASTER=M59_MLB	SYNC_DATE=06/27/2006

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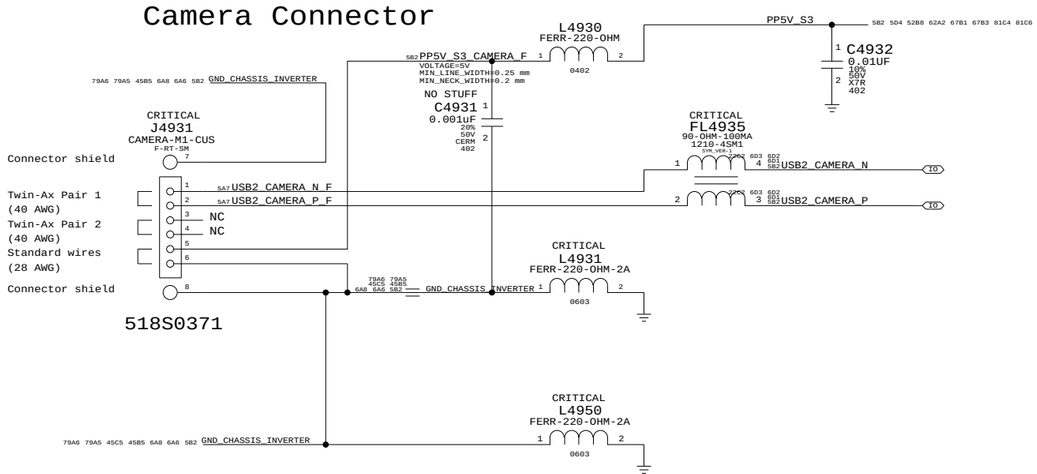
Camera Connector



Camera Connector	
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006

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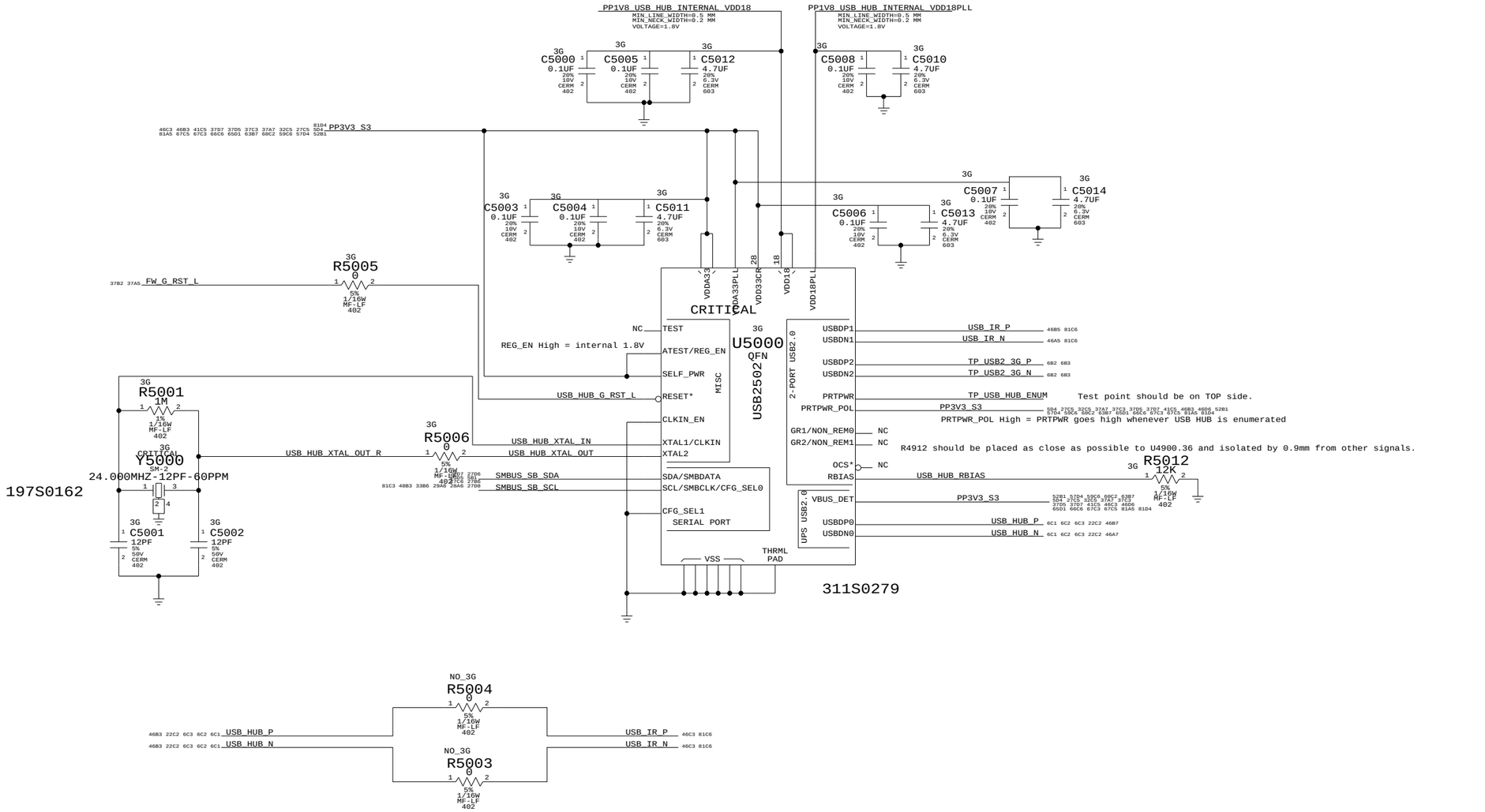

Internal USB Hub

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7164	06004
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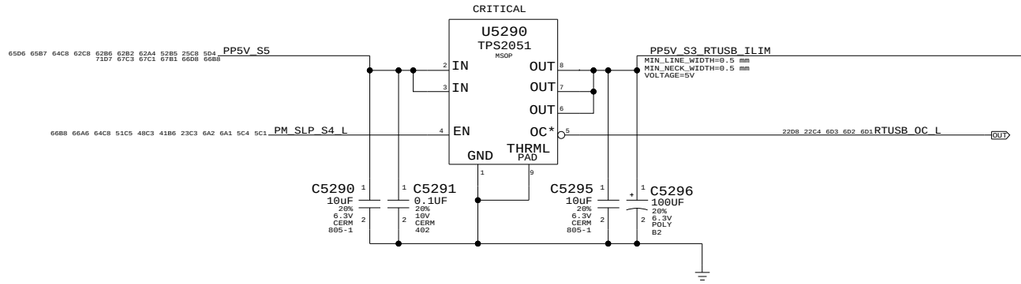
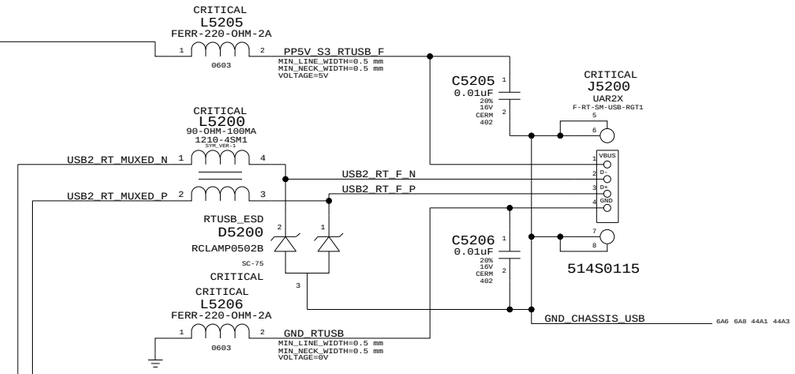
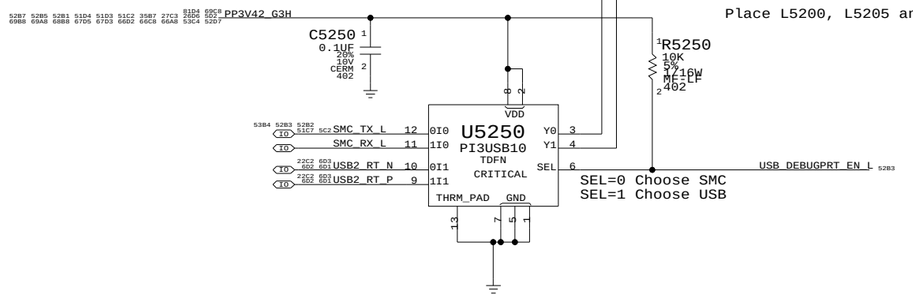
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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D	051-7164	06004

SCALE	SHT	OF
NONE	47	87

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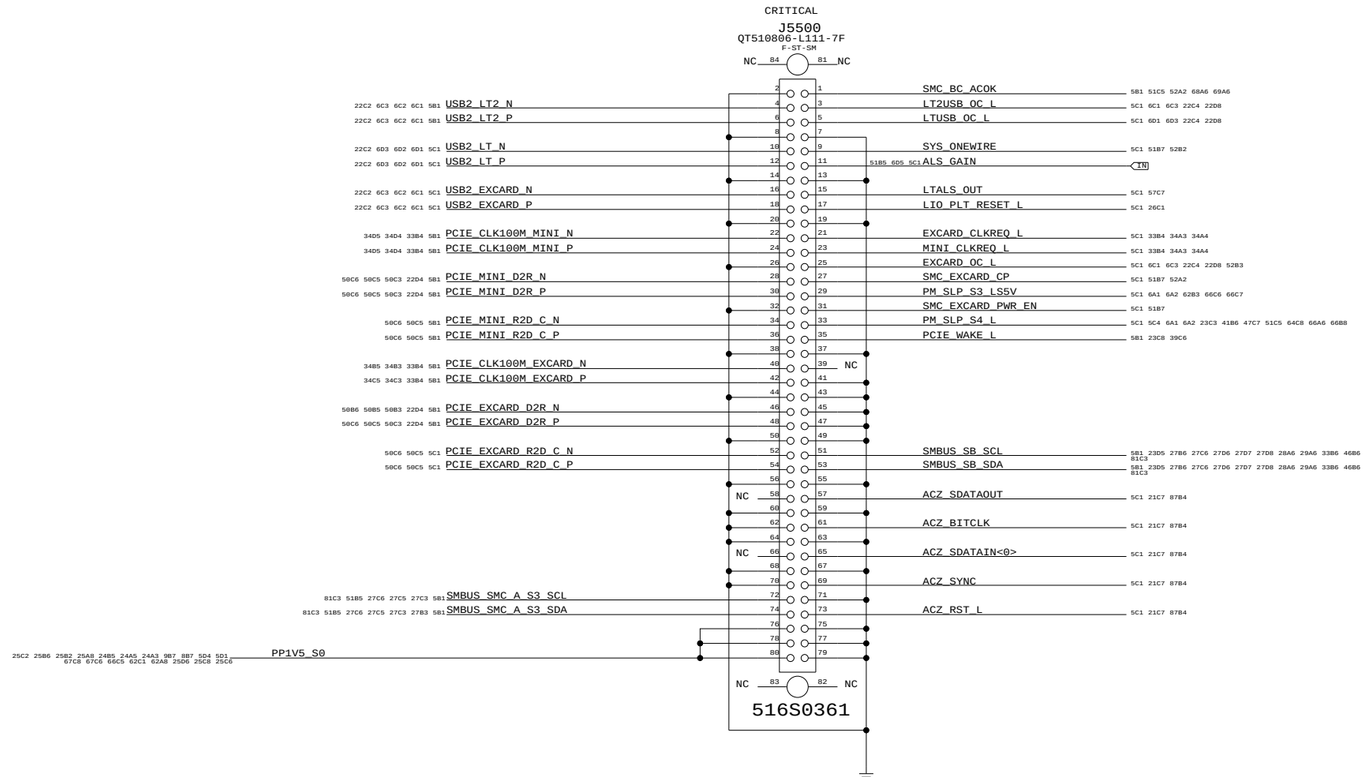
Left I/O Board Connector



Left I/O Board Connector	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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	SCALE NONE	SHT 48 OF 87	

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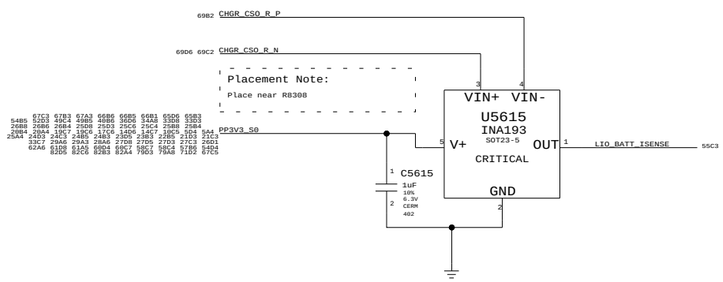
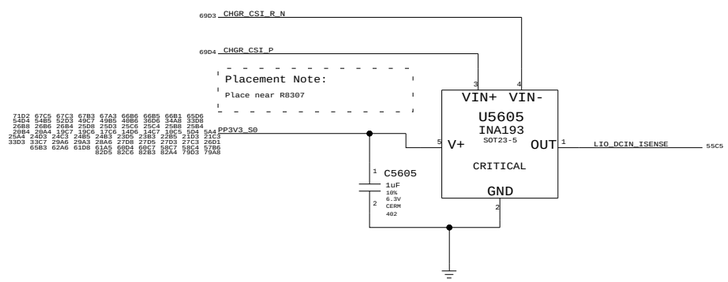
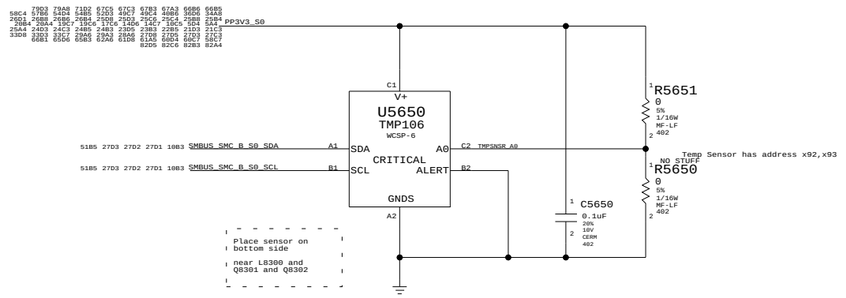
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	49	87

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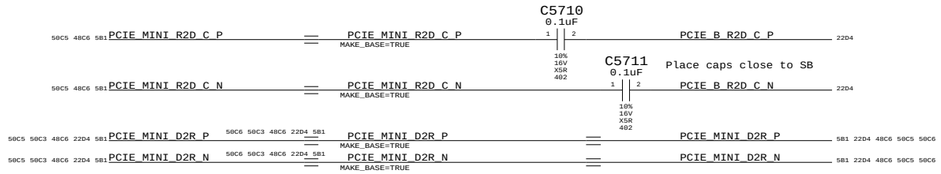
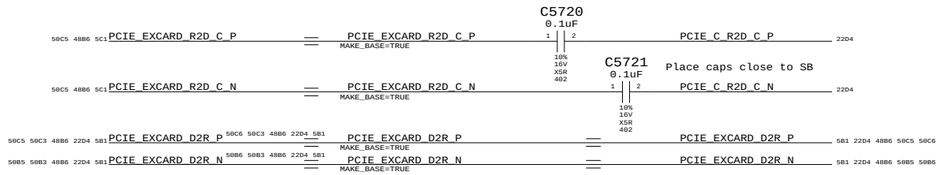
PCI-E x1 Port "A" = Ethernet (Yukon)

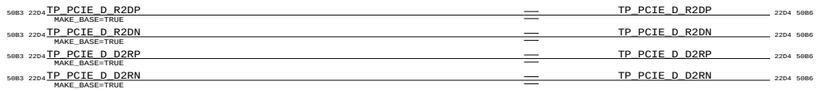
PCI-E x1 Port "B" = PCI-E Mini Card



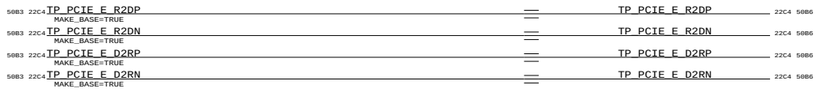
PCI-E x1 Port "C" = ExpressCard



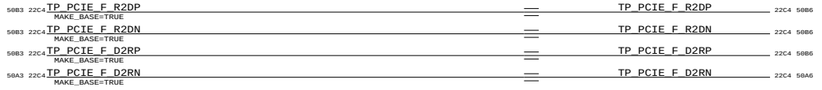
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	50	87

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UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

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	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN
	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN
	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	SPI_ARB
	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	SPI_SCLK
	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	SPI_SI
	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	SPI_SO
	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L
	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	FWH_INIT_L
	TP_SMC_P20	D13	P20	P70/AN0	N12	SMC_CPU_ISENSE
	TP_SMC_P21	D14	P21	P71/AN1	R13	SMC_CPU_VSENSE
	TP_SMC_P22	D15	P22	P72/AN2	P13	SMC_GPU_ISENSE
	TP_SMC_P23	E12	P23	P73/AN3	R14	SMC_GPU_VSENSE
	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE
	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE
	TP_SMC_P26	E13	P26	P76/AN6	N13	SMC_BATT_ISENSE
	TP_SMC_P27	F14	P27	P77/AN7	P15	SMC_P1V5S0_NB_ISENSE
	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L
	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	SMC_TPM_GPIO
	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L
	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L
	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SC_TX_L
	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SC_RX_L
	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	SMBUS_SMC_BSB_SCL
	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L
	TP_SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	SMC_BC_ACOK
	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L
	SMBUS_SMC_BSB_SDA	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L
	SMC_TPM_PP	C3	P43/TMI1/EXSCKX1	P94/IRQ13*	J4	PM_SLP_S4_L
	TP_SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L
	TP_SMC_XDP_TCK	C2	P45	P96/EXCL	H1	SMC_CLK32K_SUSCLK
	TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	SMBUS_SMC_0_S0_SDA
	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1			
	SMC_TX_L	G1	P50			
	SMC_RX_L	G4	P51			
	SMBUS_SMC_0_S0_SCL	F2	P52/SCL0			

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	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN
	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK
	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI
	SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO
	PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS
	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	TP_SMC_PF0
	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	TP_SMC_PF1
	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID
	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L
	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET
	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	TP_SMC_BATT_VSET
	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET
	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	TP_SMC_SYS_VSET
	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SPI_CE_L
	SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3
	SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	SMBUS_SMC_BSA_SDA
	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	SMBUS_SMC_BSA_SCL
	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	SMBUS_SMC_A_S3_SDA
	TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	SMBUS_SMC_A_S3_SCL
	TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	SMBUS_SMC_B_S0_SDA
	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	SMBUS_SMC_B_S0_SCL
	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT
	TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP
	TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE
	SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN
	SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	SMS_INT_L
	SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	SMS_ONOFF_L
	TP_SMC_ANALOG_ID	N11	PD3/AN11			
	SMC_P1V05S0_ISENSE	P10	PD4/AN12			
	SMC_MEM_ISENSE	R10	PD5/AN13			
	ALS_LEFT	N10	PD6/AN14			
	ALS_RIGHT	M10	PD7/AN15			

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G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

PP3V42_G3H
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS
PP3V3_AVREF_SMC

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	SMC_RST_L	E3	RES*
	SMC_XTAL	A2	XTAL
	SMC_EXTAL	B2	EXTAL
MD1		F2	SMC_MD1
MD2		K1	KBC_MDE
NMI		F4	SMC_NMI
ETRST*		L1	SMC_TRST_L
AVSS		P12, R12	

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
NOSTUFF

XW5800 SM
GND_SMC_AVSS

SMC

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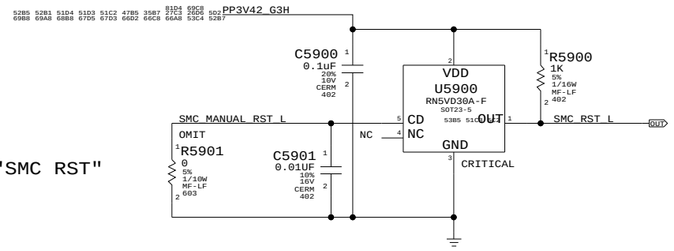
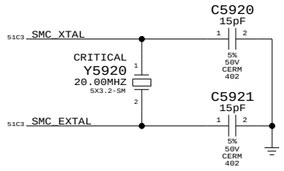
SMC Reset Button / Brownout Detect

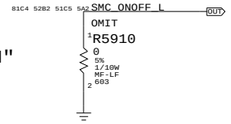


Silk: "SMC RST"

SMC Crystal Circuit

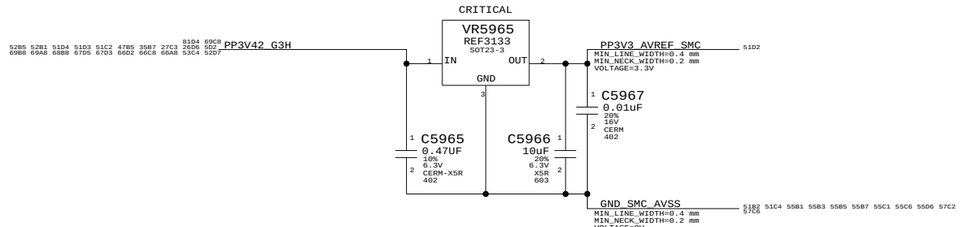


Debug Power Button

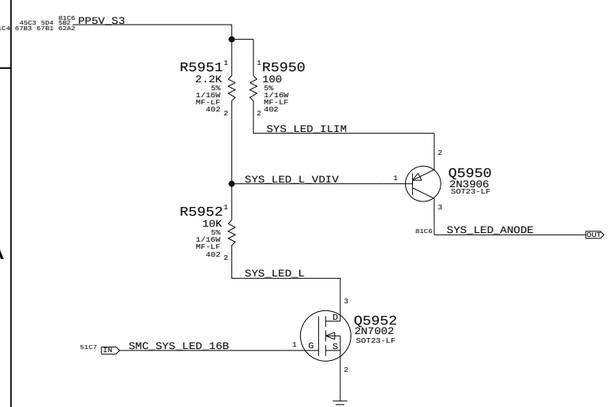


Silk: "PWR BTN"

SMC AVREF Supply

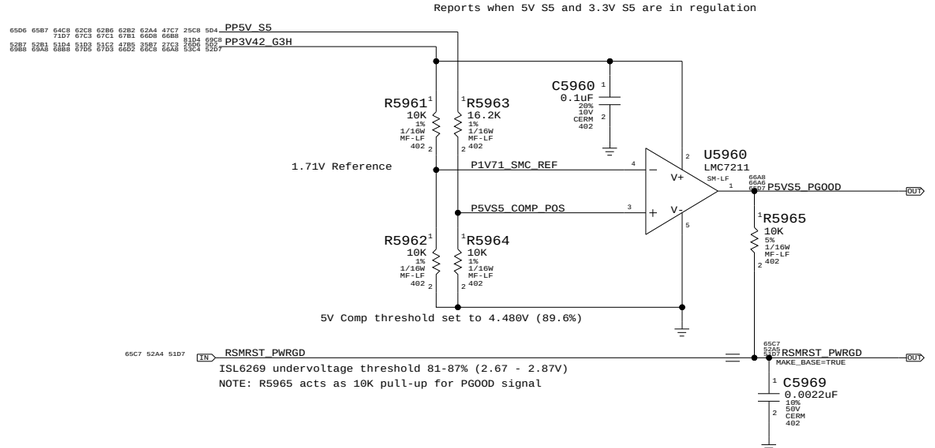


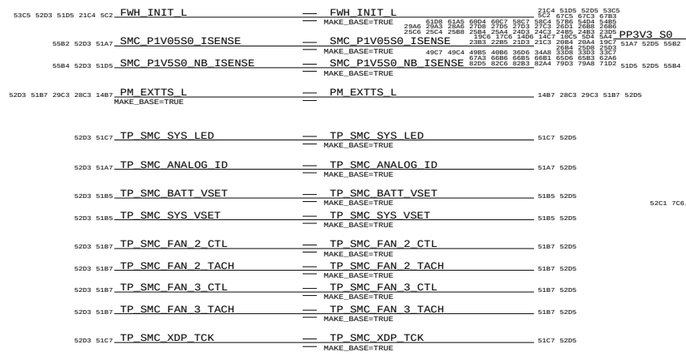
System (Sleep) LED Circuit

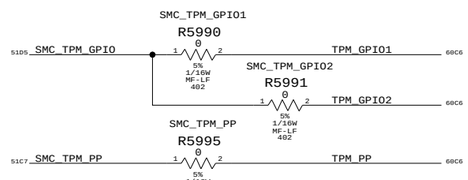


SMC PWRGD Circuit

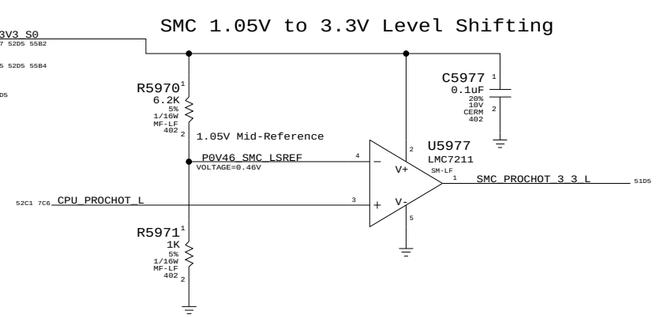
Reports when 5V S5 and 3.3V S5 are in regulation


PP5V_S5
PP3V42_G3H
R5961 10K 1% 1/16W MF-LF 402
R5963 16.2K 1% 1/16W MF-LF 402
C5960 0.1uF 20% 10V CERM 402
1.71V Reference
P1V71_SMC_REF
P5VS5_COMP_POS
R5962 10K 1% 1/16W MF-LF 402
R5964 10K 1% 1/16W MF-LF 402
U5960 LMC7211 SM-LF
P5VS5_PGOOD
R5965 10K 5% 1/16W MF-LF 402
5V Comp threshold set to 4.480V (89.6%)
RSMRST_PWRGD
ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal
C5969 0.0022uF 10% 50V CERM 402

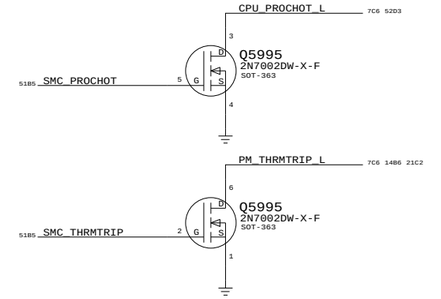


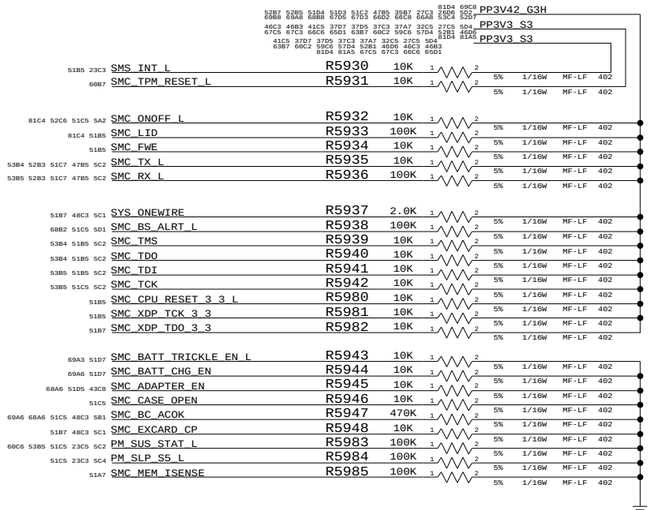


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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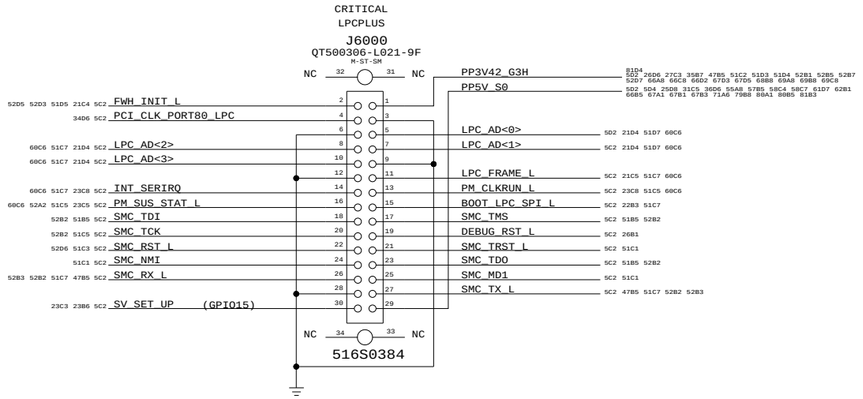

LPC+ Debug Connector

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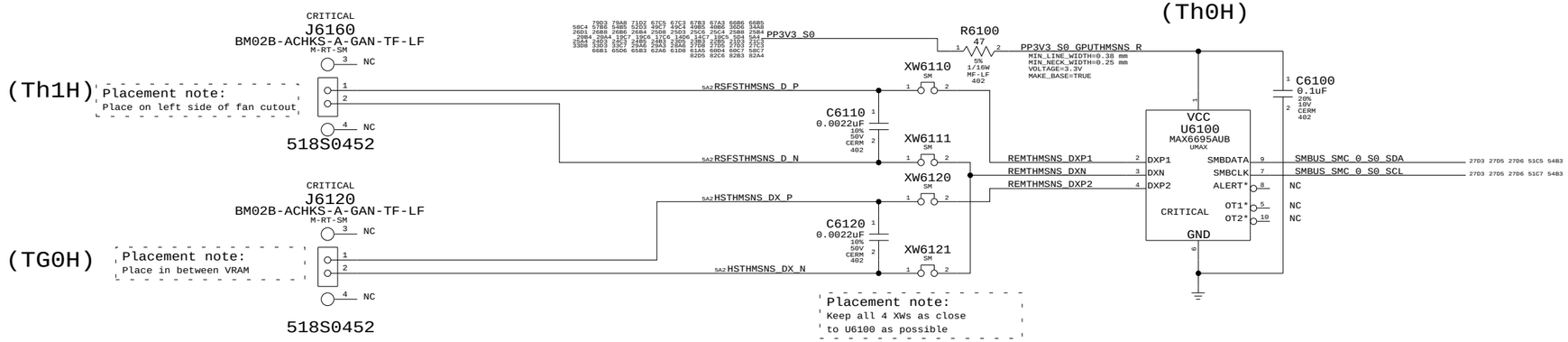
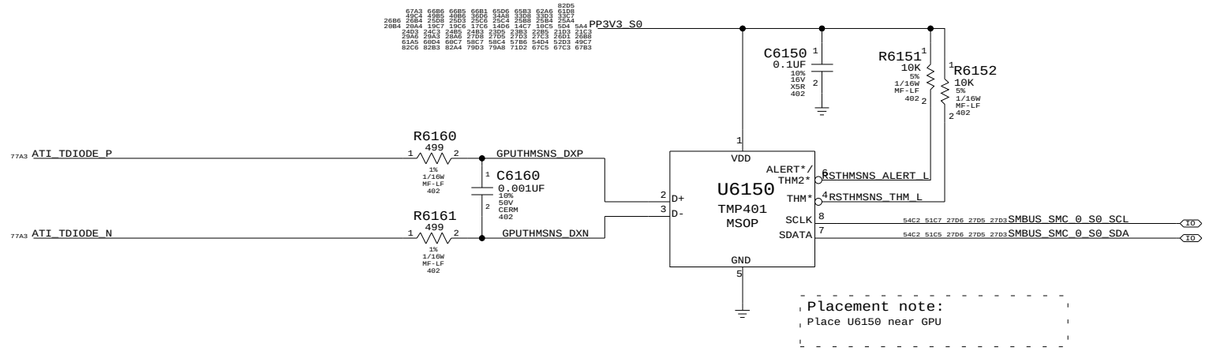
GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

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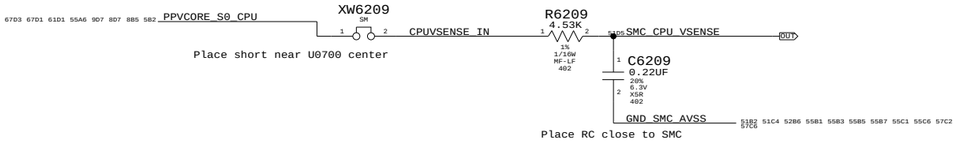
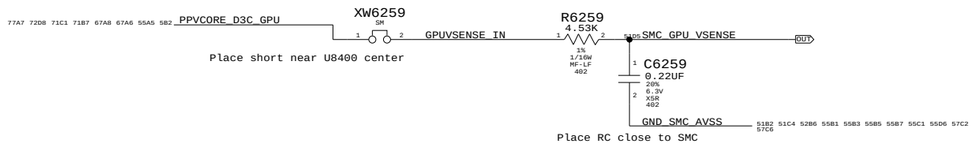
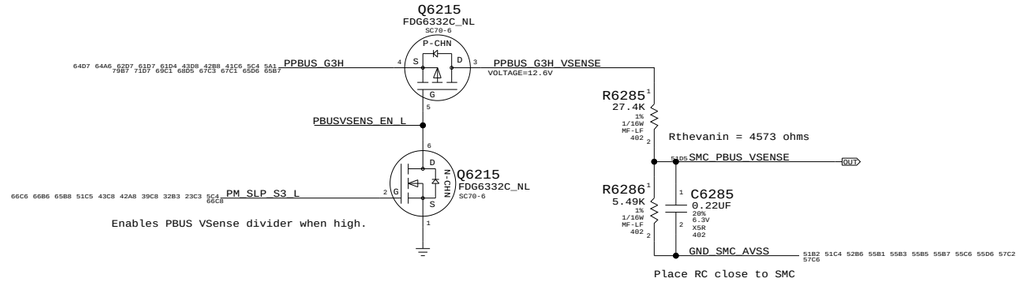
CPU Voltage Sense / Filter



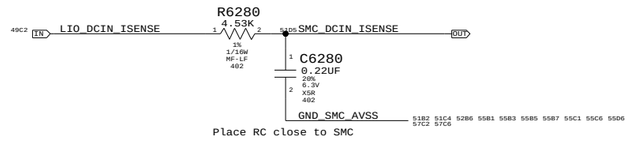
GPU Voltage Sense / Filter



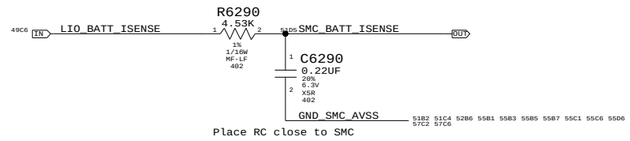
PBUS Voltage Sense Enable & Filter



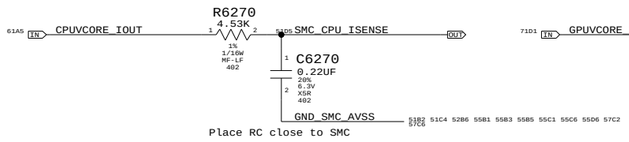
DCIN Current Sense Filter



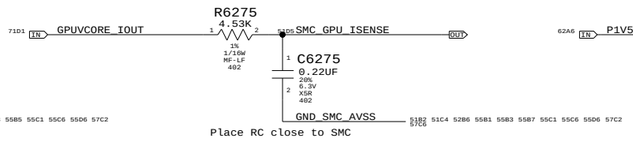
Battery Current Sense Filter



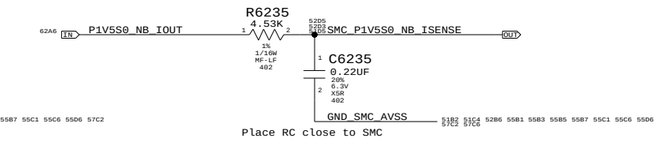
CPU Current Sense Filter



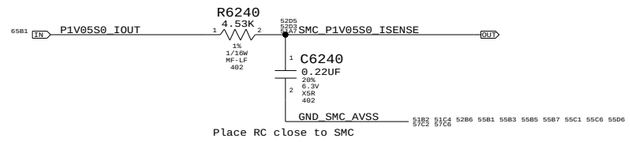
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

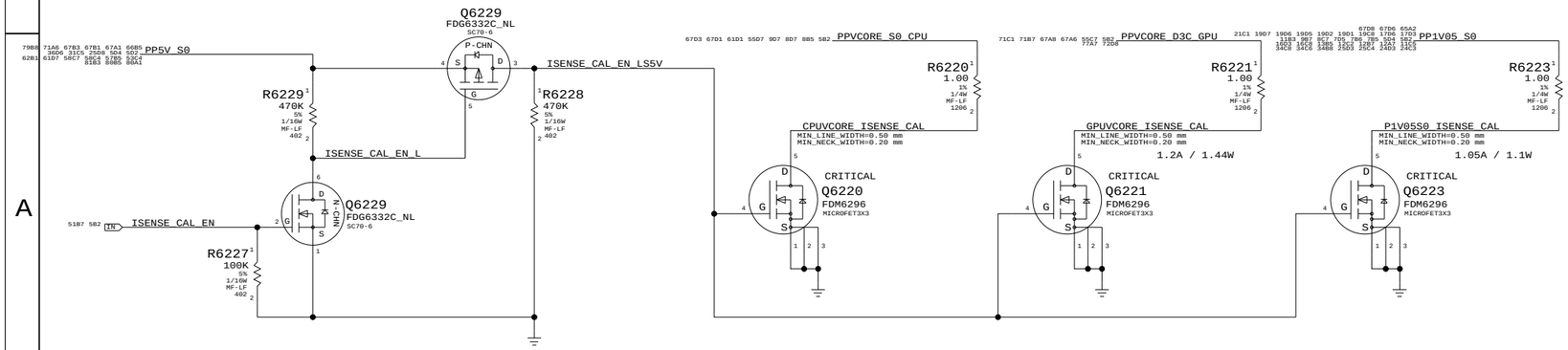


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

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SCALE	SHT	OF
NONE	55	87

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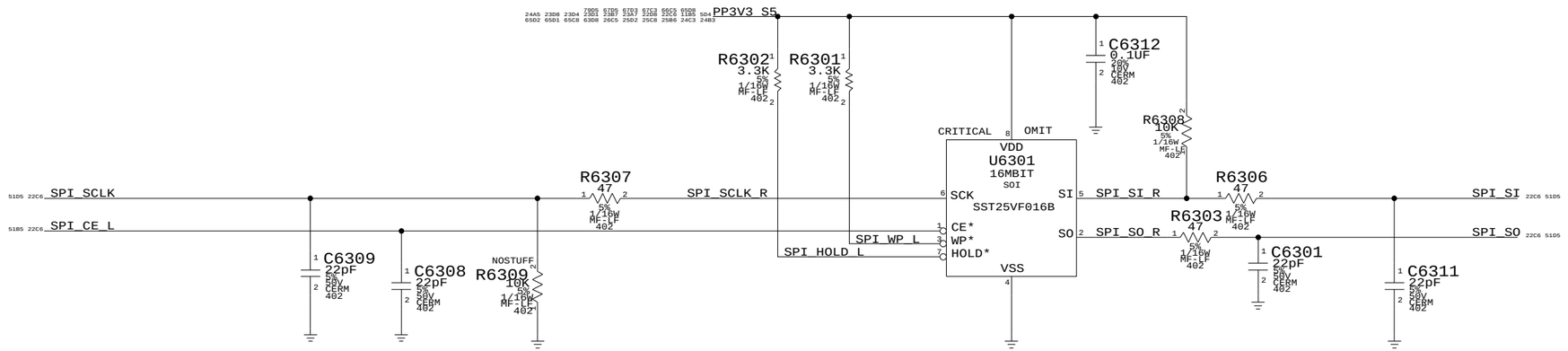

R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

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SCALE NONE SHT 56 OF 87

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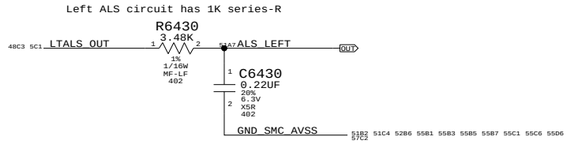
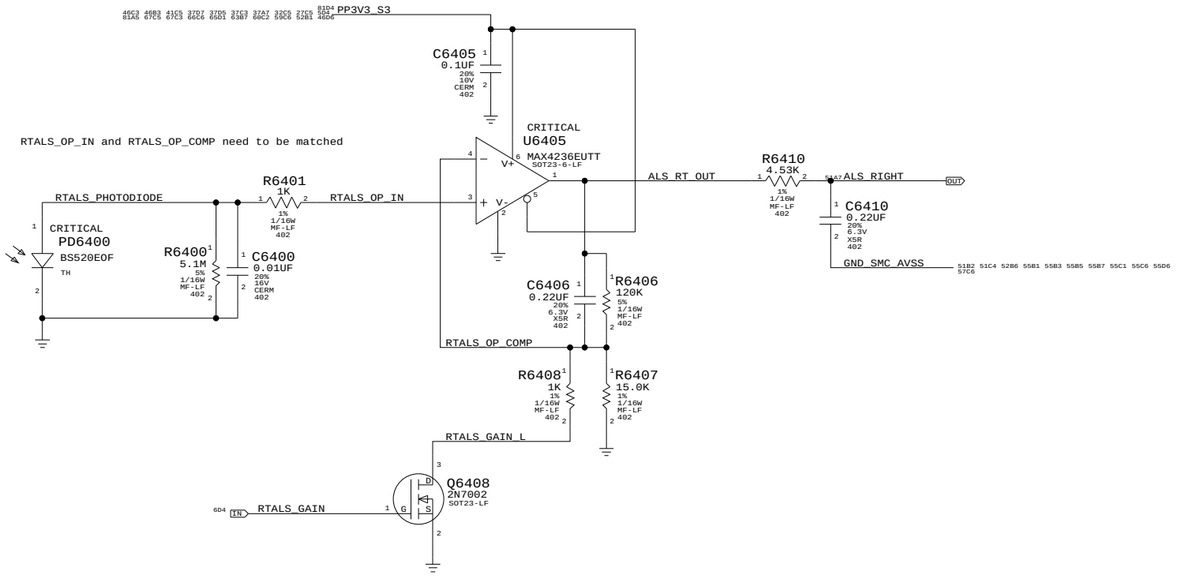
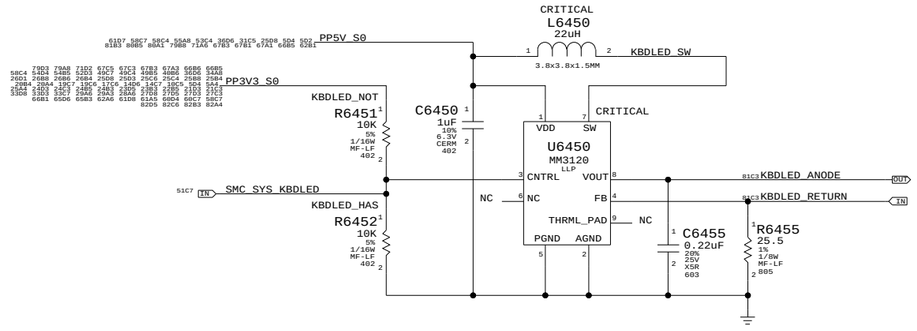
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	57	87

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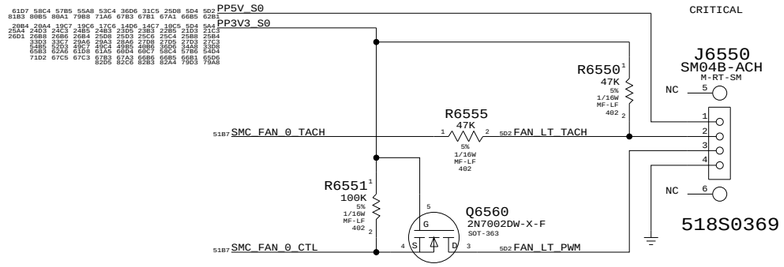
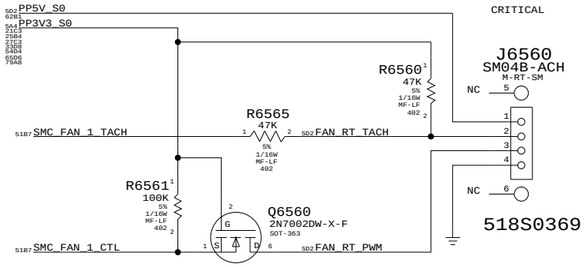
Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7164	06004

SCALE	SHT	OF
NONE	58	87

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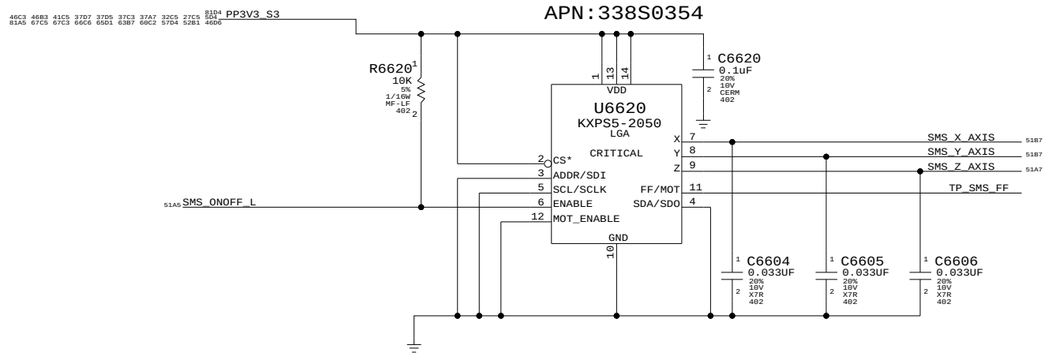
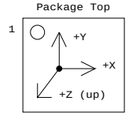
APN:338S0354



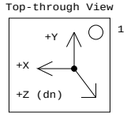
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

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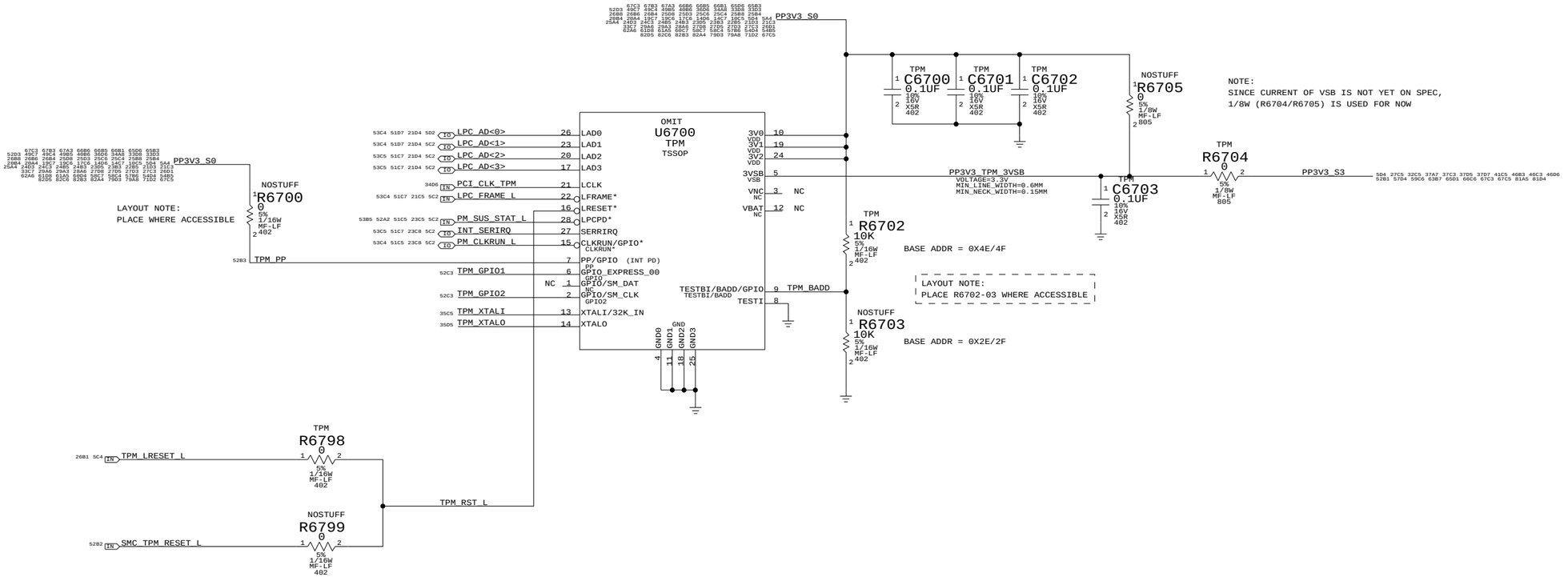

TPM		
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006	

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	SCALE: NONE	SHT 60 OF 87	

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DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

NO STUFF
C7501
0.0022UF
10%
50V
CERM
402

NO STUFF
C7502
0.0022UF
10%
50V
CERM
402

NO STUFF
C7551
0.0022UF
10%
50V
CERM
402

NO STUFF
C7552
0.0022UF
10%
50V
CERM
402

NO STUFF
C7581
0.01uF
10%
16V
CERM
402

NO STUFF
C7542
0.001uF
10%
50V
CERM
402

NO STUFF
R7536
2.0K
1%
1/16W
MF-LF
402

NO STUFF
C7594
0.1uF
20%
10V
CERM
402

CPU VCore Current Sense

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)

Voffset = (Vdrp_offset * Kdroop) + Vamp_offset

Gain = Rc / (Ra + Rb)

Voffset worst-case ~2.3mV (+/- ~1A offset)

Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

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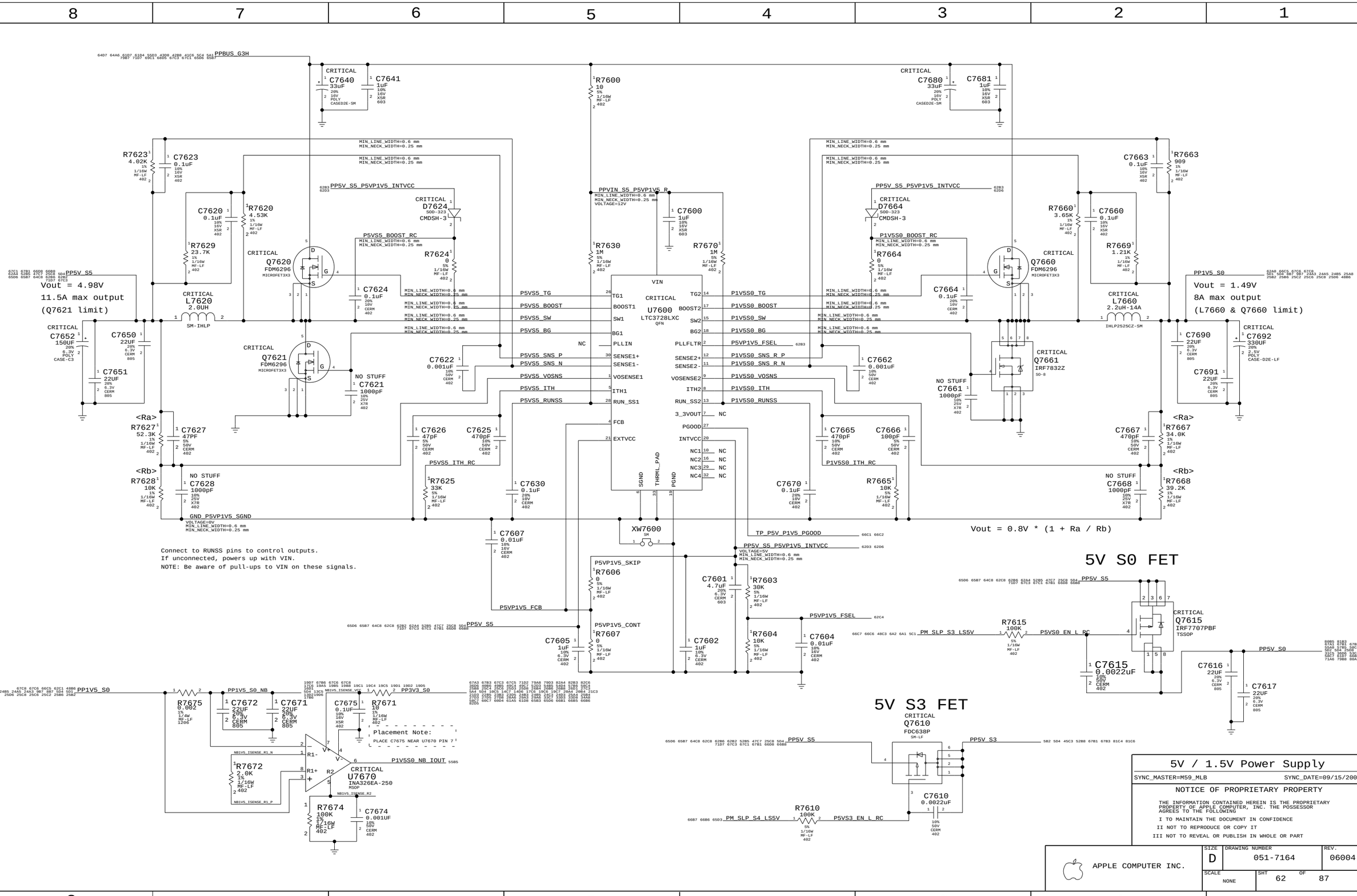

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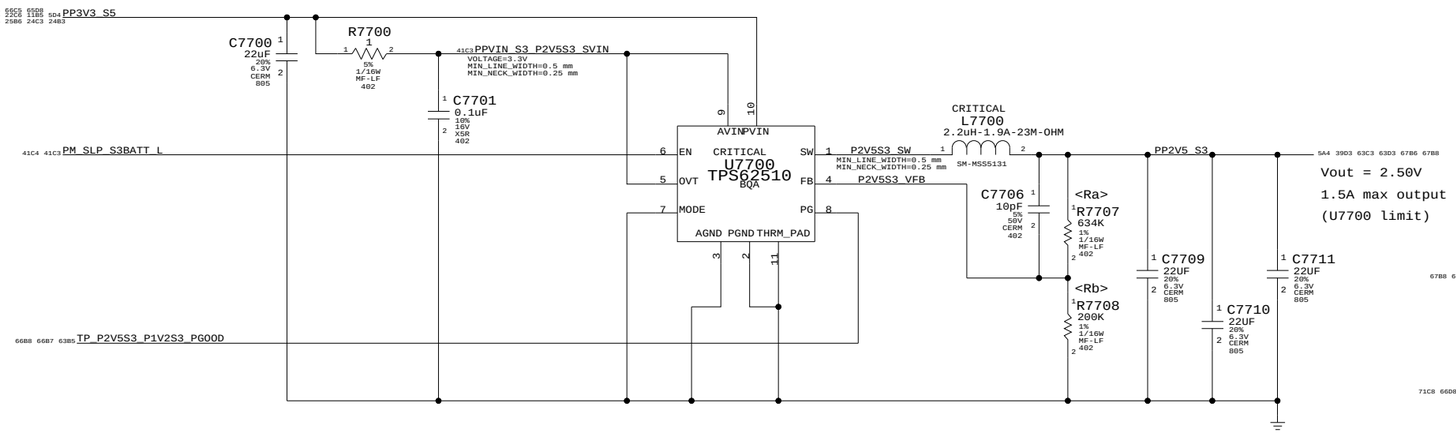
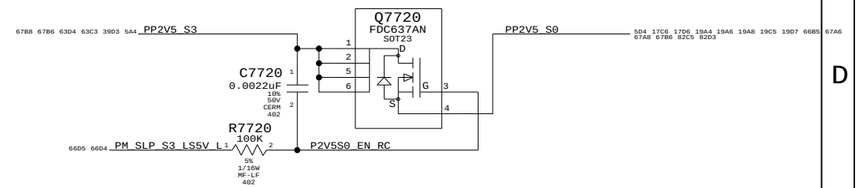
2.5V S3 Regulator



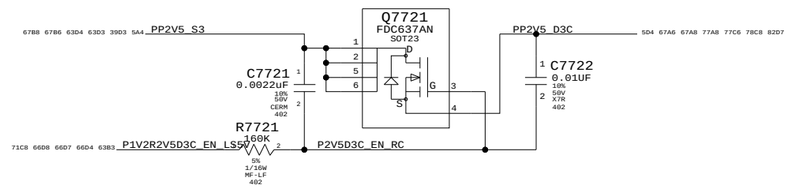
Vout = 2.50V
1.5A max output
(U7700 limit)

Vout = 0.6V * (1 + Ra / Rb)

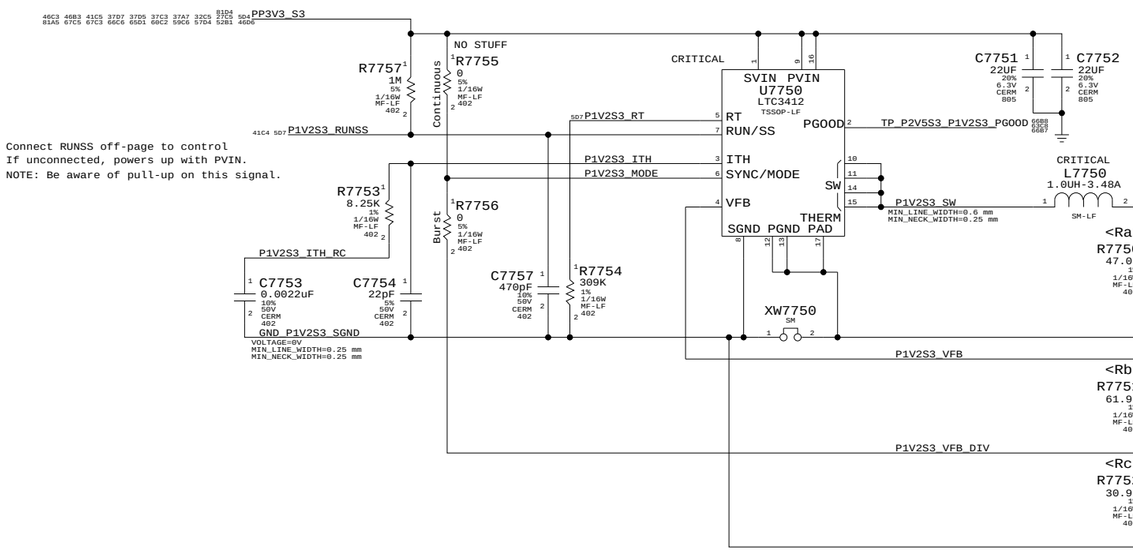
2.5V S0 FET



2.5V D3Cold FET



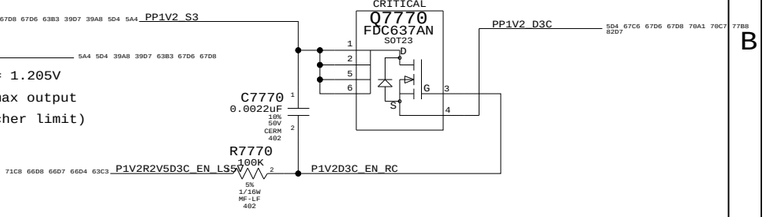
1.2V S3 Regulator



Vout = 0.8V * (1 + Ra / (Rb + Rc))

Vout = 1.205V
2.5A max output
(Switcher limit)

1.2V D3Cold FET



2.5V & 1.2V Regulators	
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006

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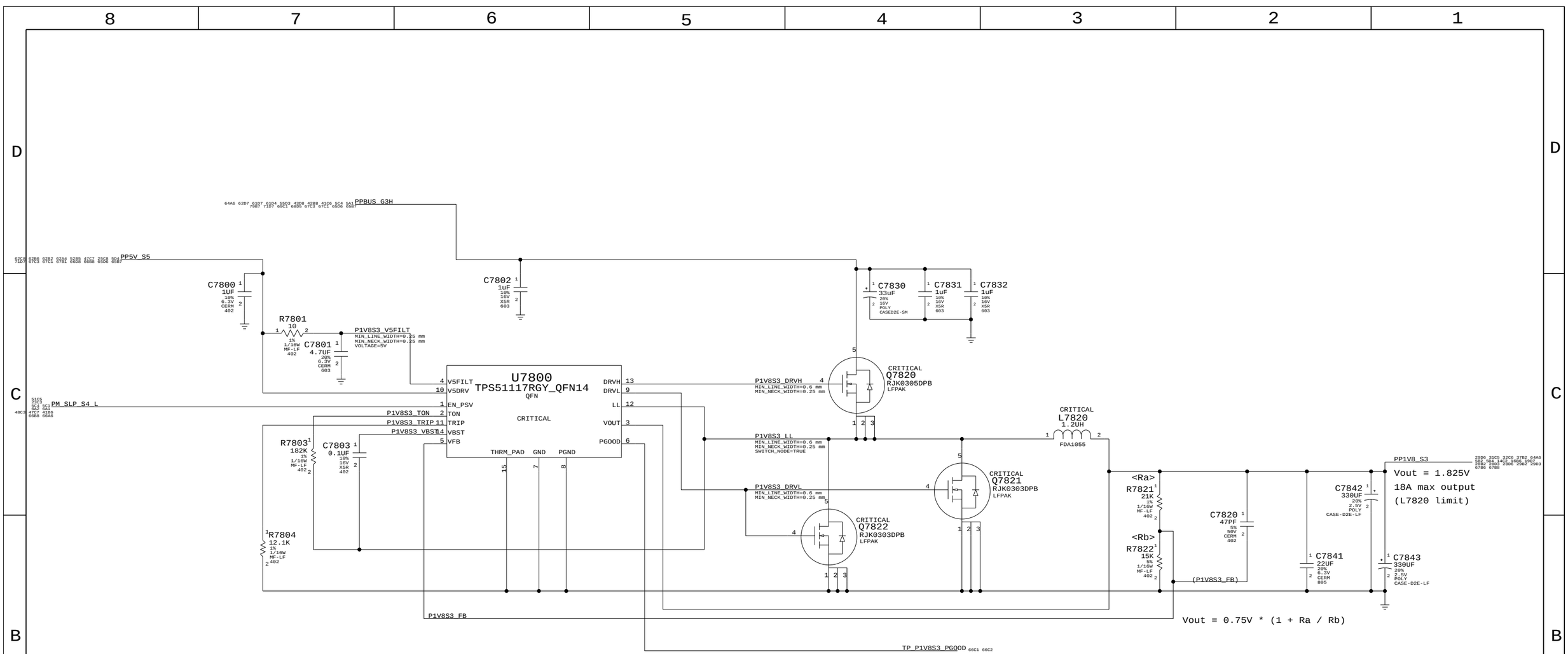
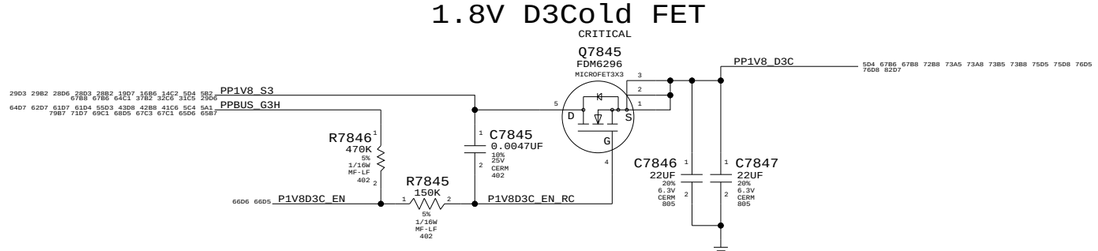


1.8V D3Cold FET



1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	64	87

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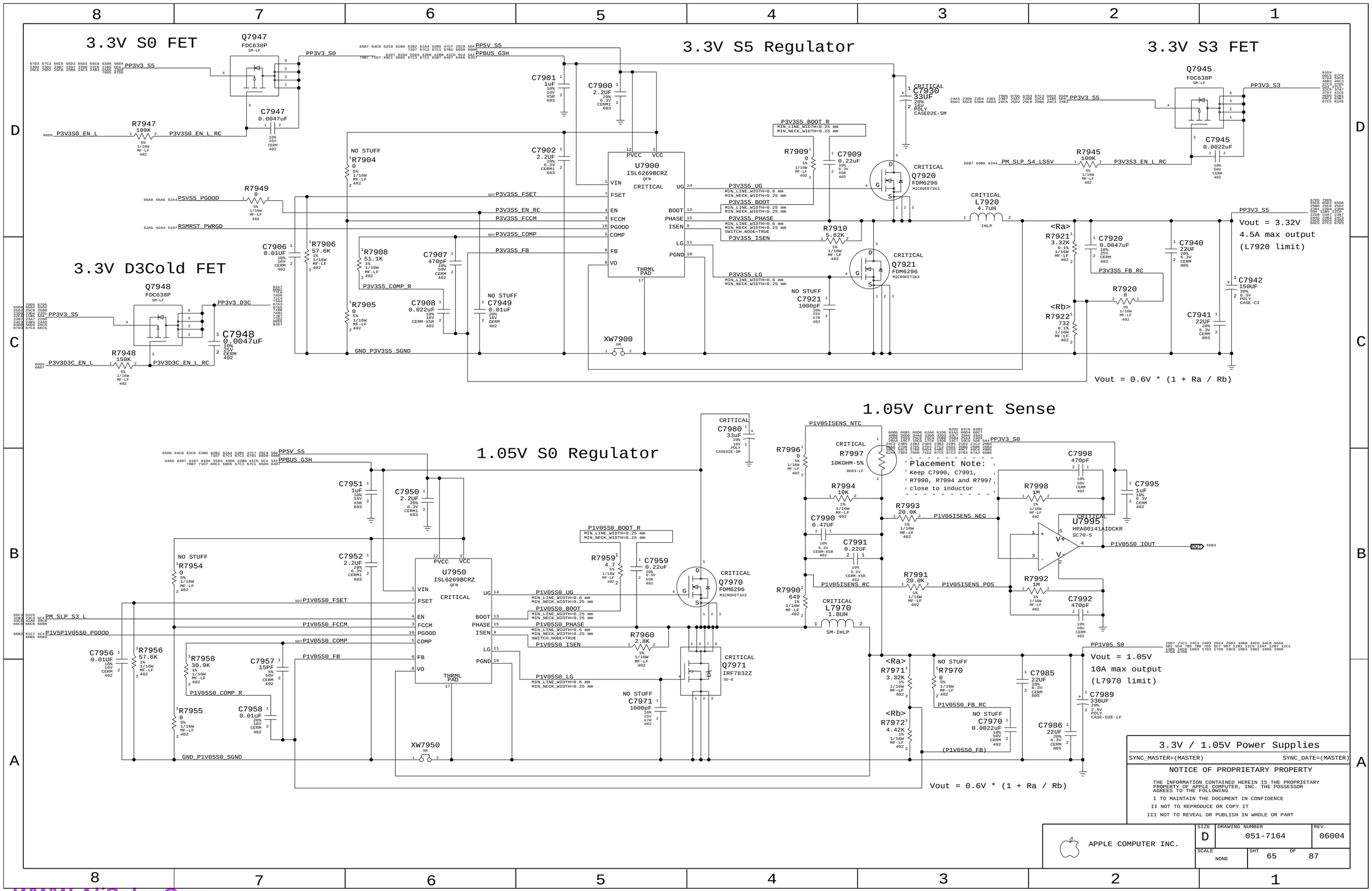

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Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PP5V_S5

R8050 10K 5% 1/16W MF-LF 402

R8051 10K 5% 1/16W MF-LF 402

R8052 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

R8068 10K 5% 1/16W MF-LF 402

R8069 10K 5% 1/16W MF-LF 402

IN P1V2R2V5D3C_EN_LS5V

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V MAKE_BASE=TRUE

P1V2R2V5D3C_EN_LS5V

P1V2R2V5D3C_EN_LS5V

P3V3D3C_EN_L MAKE_BASE=TRUE

P3V3D3C_EN_L

P1V8D3C_EN MAKE_BASE=TRUE

P1V8D3C_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363

Q8056 2N7002DW-X-F SOT-363

Q8050 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V_L MAKE_BASE=TRUE

PM_SLP_S3_LS5V_L

P3V3S0_EN_L MAKE_BASE=TRUE

P3V3S0_EN_L

Q8058 2N7002DW-X-F SOT-363

Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V MAKE_BASE=TRUE

PM_SLP_S3_LS5V

PM_SLP_S3_LS5V

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363

R8054 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

IN PM_SLP_S3_L

R8056 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PP3V3_S3

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

(PM_SLP_S3_L) MAKE_BASE=TRUE

PP3V3_S0

R8053 10K 5% 1/16W MF-LF 402

R8081 10K 5% 1/16W MF-LF 402

C8081 0.1uF 20% 10V CERM 402

PM_SLP_S3_L_GPUVCORE_EN

U8081 MC74VHC1G08 SC70

C8053 0.047UF 10% 10V CERM 402

SB_GPUVCORE_DISABLE_L

SB_GPUVCORE_DISABLE_L MAKE_BASE=TRUE

GPUVCORE_EN

GPUVCORE_EN MAKE_BASE=TRUE

GPUVCORE_EN

IN TP_P2V5S3_P1V2S3_PGOOD

IN TP_P2V5S3_P1V2S3_PGOOD

TP_P2V5S3_P1V2S3_PGOOD MAKE_BASE=TRUE

This signal was used as an option previously to test for 2v5 and 1v2 S3 valid for GPUVCORE_EN. But was disconnected for C8053 placement.

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

PP5V_S5

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V MAKE_BASE=TRUE

PM_SLP_S4_LS5V

PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

IN PM_SLP_S4_L

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) MAKE_BASE=TRUE

PM_SLP_S4_L

PM_SLP_S4_L

PM_SLP_S4_L

PP3V42_G3H

IN P5VS5_PGOOD

(P5VS5_PGOOD) MAKE_BASE=TRUE

P5VS5_PGOOD

P5VS5_RUNSS

5V Enable has pull-up to PBUS

R8059 470K 5% 1/16W MF-LF 402

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

IN SMC_PM_G2_EN

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

C8000 10UF 10% 25V X5R 1206-1

U8000 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC NC CRITICAL FB GND

P3V42G3H5_BOOST

P3V42G3H_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

P3V42G3H_FB

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402

<Rb> R8011 200K 1% 1/16W MF-LF 402

PP3V42_G3H

Vout = 3.425

200mA max output

(Switcher limit)

C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5

PP1V5_S0

R8061 27.4K 1% 1/16W MF-LF 402

R8063 4.99K 1% 1/16W MF-LF 402

0.89V Reference

P1V0_P1V5PG_REF

P1V5S0_COMP_POS

R8062 10K 1% 1/16W MF-LF 402

R8064 10K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

U8060 LMC7211 SM-LF

P1V5S0_PGOOD

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5S0_PGOOD

P1V5P1V05S0_PGOOD

P1V5P1V05S0_PGOOD MAKE_BASE=TRUE

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)

NOTE: R8065 acts as 10K pull-up for PGOOD signal

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

PP3V3_S0

PP5V_S0

PP2V5_S0

PP0V9_S0

R8074 68.1K 1% 1/16W MF-LF 402

R8072 365K 1% 1/16W MF-LF 402

R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

U8070 LTC2903 TSOT-23

CRITICAL

S0PGOOD_5V_DIV

S0PGOOD_2V5_DIV

S0PGOOD_0V9_DIV

RST*

GND

R8076 10K 5% 1/16W MF-LF 402

S0PGOOD_PWROK

R8075 100K 1% 1/16W MF-LF 402

C8075 0.1UF 20% 10V CERM 402

R8073 100K 1% 1/16W MF-LF 402

C8073 0.1UF 20% 10V CERM 402

R8071 100K 1% 1/16W MF-LF 402

C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD MAKE_BASE=TRUE

TP_P5V_P1V5_PGOOD

TP_P1V8S3_PGOOD MAKE_BASE=TRUE

TP_P1V8S3_PGOOD

PP3V3_S0

MC74VHC1G08 SC70

U8080

ALL_SYS_PWRGD

PGOOD_MUXED_S0_OR_S0D3C

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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DC-In Connector

CRITICAL

J8290
87438-0832-BLK
M-RT-SM

PPBUS_G3H
9A1 9C4 41C6 42B8 43D8 55D3 61D4 61D7 62D7 64A6 64D7 65B7 65D6 67C1 67C3 69C1 71D7 79B7

PP18V5_DCIN
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.60mm
MIN_NECK_WIDTH=0.20mm
5B1 68B8

518S0456

D8201
1SS355
SOD-323

PPDCIN_G3H_R
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm

R8207
47
5%
1/8W
MF-LF
805

PPDCIN_G3H
66D5 67A6 67A8 69B2

Inrush Limiter

CRITICAL

Q8250
SI4405DY-E3
SO-8

PP18V5_G3H_CHGR
68B3 69D8

R8221
470K
1%
1/10W
MF-LF
402

C8250
0.22uF
20%
25V
X5R
603

ACIN_ENABLE_DIV_L
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm

R8250
330K
5%
1/10W
MF-LF
402

ACIN_ENABLE_DIV2_L

Q8210
2N7002
SOT23-LF

U8250
MC74VHC1G08
SC70

ACOK_AND_PS_ON

ACIN Detection

PP18V5_DCIN
68C5 5B1

PP3V42_G3H
69C8 69B8 69A8 68B8 67D5 53C4 52D7 52B7 52B6 66D2 66C8 66A8 53C4 52D7 52B7 52B5 52B1 5104 5103 51C2 27B5 39A7 27C5 26D6 46C2

<R1b>
R8212
102K
1%
1/16W
MF-LF
402

<R1a>
R8214
102K
1%
1/16W
MF-LF
402

ACIN_1V20_REF

<R2b>
R8213
10.7K
1%
1/16W
MF-LF
402

<R2a>
R8215
57.6K
1%
1/16W
MF-LF
402

ACIN_DIV

C8210
0.1uF
20%
25V
CERM
402

52A2 51D5 43C8 SMC_ADAPTER_EN

CRITICAL

U8200
LMC7211
SM-LF

R8216
1M
5%
1/16W
MF-LF
402

SMC_BC_ACOK
5B1 48C3 51C5 52A2 69A6

NOTE: R8210 is on M57 LIO!

System must provide 10K-70K impedance
to A52 adapter for system load detection.
REQ of R8210 (on M57 LIO), R8212, & R8213 is 36.9K.

Vref = 3.42V * (R2a / (R1a + R2a))
Vth = (Vref / (R2b / (R1b + R2b))

Vref = 1.23V

Vth = 13.0V

Assuming 1% variance for R8210-R8215 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

Battery Connector

CRITICAL

J8250
87438-1043-BLK
M-RT-SM

BATT_NEG
SMC_BS_ALRT_L
SMBUS_SMC_BSA_SDA
SMBUS_SMC_BSA_SCL
(HOST_DETECT_L)
BATT_POS
69B1 68A1

BATT_NEG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
5D1 68B2

GND

BATT_POS
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
5D1 68A1 68A2 69B1

518S0457

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PBus Supply & Battery Charger

Battery Charge FET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R8304		ISL6257H

PBus Supply & Batt. Charger

SYNC_MASTER=M59_LIO SYNC_DATE=09/15/2006

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SCALE: NONE	SHT 69 OF 87	

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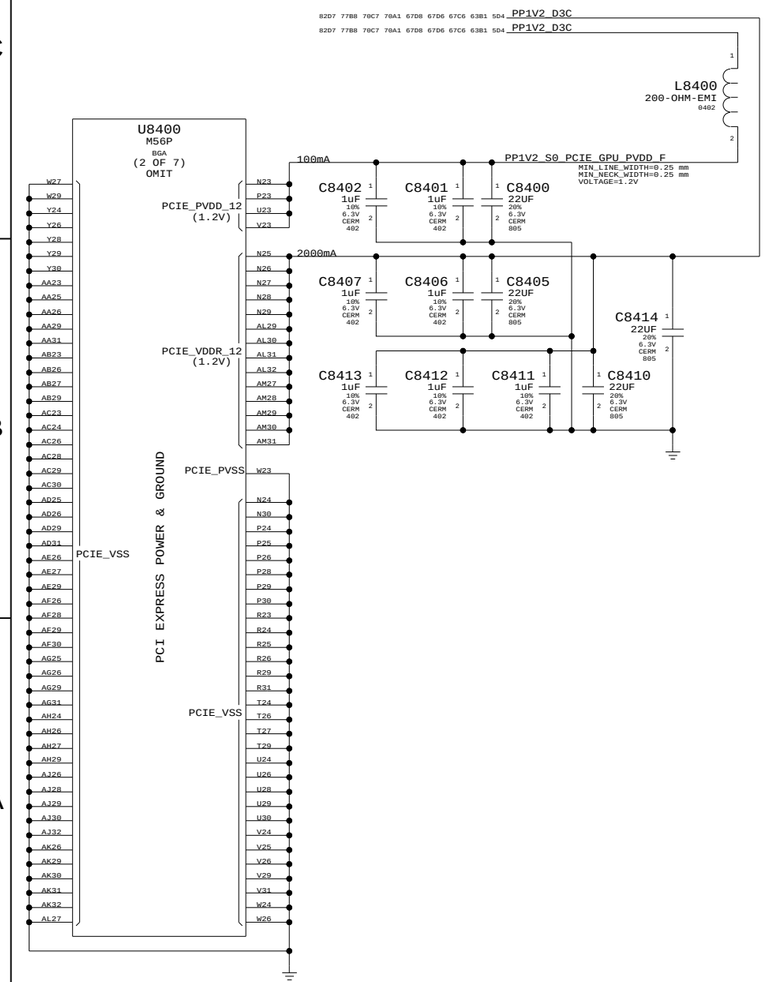

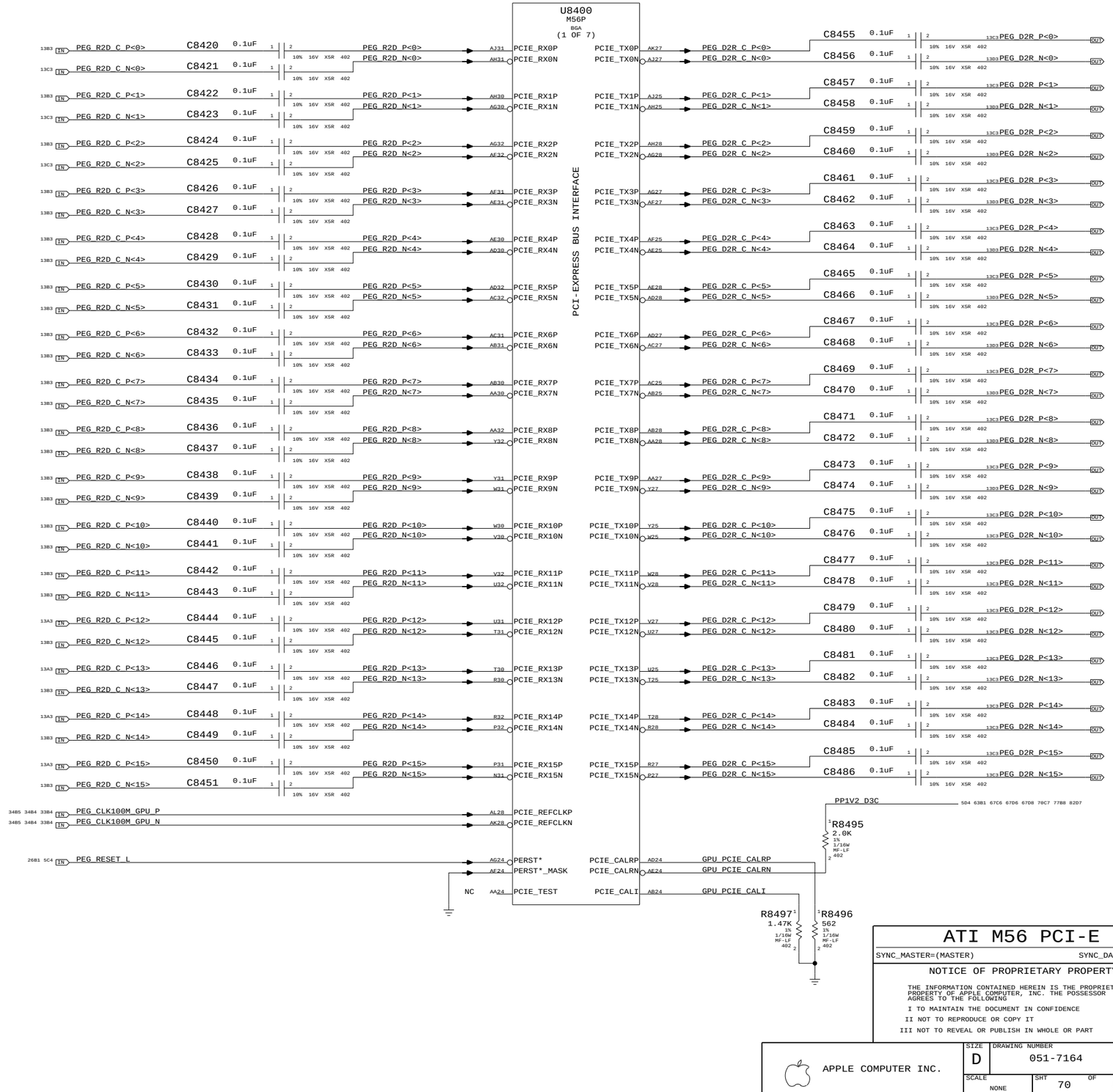
OMIT
U8400
M56P
BGA
(1 OF 7)
PCI-EXPRESS BUS INTERFACE
PEG_R2D_C_P<0> C8420 0.1uF PEG_R2D_P<0> AJ31 PCIE_RX0P
PEG_R2D_C_N<0> C8421 0.1uF PEG_R2D_N<0> AH31 PCIE_RX0N
PEG_R2D_C_P<1> C8422 0.1uF PEG_R2D_P<1> AH30 PCIE_RX1P
PEG_R2D_C_N<1> C8423 0.1uF PEG_R2D_N<1> AG30 PCIE_RX1N
PEG_R2D_C_P<2> C8424 0.1uF PEG_R2D_P<2> AG32 PCIE_RX2P
PEG_R2D_C_N<2> C8425 0.1uF PEG_R2D_N<2> AF32 PCIE_RX2N
PEG_R2D_C_P<3> C8426 0.1uF PEG_R2D_P<3> AF31 PCIE_RX3P
PEG_R2D_C_N<3> C8427 0.1uF PEG_R2D_N<3> AE31 PCIE_RX3N
PEG_R2D_C_P<4> C8428 0.1uF PEG_R2D_P<4> AE30 PCIE_RX4P
PEG_R2D_C_N<4> C8429 0.1uF PEG_R2D_N<4> AD30 PCIE_RX4N
PEG_R2D_C_P<5> C8430 0.1uF PEG_R2D_P<5> AD32 PCIE_RX5P
PEG_R2D_C_N<5> C8431 0.1uF PEG_R2D_N<5> AC32 PCIE_RX5N
PEG_R2D_C_P<6> C8432 0.1uF PEG_R2D_P<6> AC31 PCIE_RX6P
PEG_R2D_C_N<6> C8433 0.1uF PEG_R2D_N<6> AB31 PCIE_RX6N
PEG_R2D_C_P<7> C8434 0.1uF PEG_R2D_P<7> AB30 PCIE_RX7P
PEG_R2D_C_N<7> C8435 0.1uF PEG_R2D_N<7> AA30 PCIE_RX7N
PEG_R2D_C_P<8> C8436 0.1uF PEG_R2D_P<8> AA32 PCIE_RX8P
PEG_R2D_C_N<8> C8437 0.1uF PEG_R2D_N<8> Y32 PCIE_RX8N
PEG_R2D_C_P<9> C8438 0.1uF PEG_R2D_P<9> Y31 PCIE_RX9P
PEG_R2D_C_N<9> C8439 0.1uF PEG_R2D_N<9> W31 PCIE_RX9N
PEG_R2D_C_P<10> C8440 0.1uF PEG_R2D_P<10> W30 PCIE_RX10P
PEG_R2D_C_N<10> C8441 0.1uF PEG_R2D_N<10> V30 PCIE_RX10N
PEG_R2D_C_P<11> C8442 0.1uF PEG_R2D_P<11> V32 PCIE_RX11P
PEG_R2D_C_N<11> C8443 0.1uF PEG_R2D_N<11> U32 PCIE_RX11N
PEG_R2D_C_P<12> C8444 0.1uF PEG_R2D_P<12> U31 PCIE_RX12P
PEG_R2D_C_N<12> C8445 0.1uF PEG_R2D_N<12> T31 PCIE_RX12N
PEG_R2D_C_P<13> C8446 0.1uF PEG_R2D_P<13> T30 PCIE_RX13P
PEG_R2D_C_N<13> C8447 0.1uF PEG_R2D_N<13> R30 PCIE_RX13N
PEG_R2D_C_P<14> C8448 0.1uF PEG_R2D_P<14> R32 PCIE_RX14P
PEG_R2D_C_N<14> C8449 0.1uF PEG_R2D_N<14> P32 PCIE_RX14N
PEG_R2D_C_P<15> C8450 0.1uF PEG_R2D_P<15> P31 PCIE_RX15P
PEG_R2D_C_N<15> C8451 0.1uF PEG_R2D_N<15> N31 PCIE_RX15N
PEG_CLK100M_GPU_P AL28 PCIE_REFCLKP
PEG_CLK100M_GPU_N AK28 PCIE_REFCLKN
PEG_RESET_L AG24 PERST*
AF24 PERST*_MASK
NC AA24 PCIE_TEST
PCIE_TX0P AK27 PEG_D2R_C_P<0> C8455 0.1uF PEG_D2R_P<0>
PCIE_TX0N AJ27 PEG_D2R_C_N<0> C8456 0.1uF PEG_D2R_N<0>
PCIE_TX1P AJ25 PEG_D2R_C_P<1> C8457 0.1uF PEG_D2R_P<1>
PCIE_TX1N AH25 PEG_D2R_C_N<1> C8458 0.1uF PEG_D2R_N<1>
PCIE_TX2P AH28 PEG_D2R_C_P<2> C8459 0.1uF PEG_D2R_P<2>
PCIE_TX2N AG28 PEG_D2R_C_N<2> C8460 0.1uF PEG_D2R_N<2>
PCIE_TX3P AG27 PEG_D2R_C_P<3> C8461 0.1uF PEG_D2R_P<3>
PCIE_TX3N AF27 PEG_D2R_C_N<3> C8462 0.1uF PEG_D2R_N<3>
PCIE_TX4P AF25 PEG_D2R_C_P<4> C8463 0.1uF PEG_D2R_P<4>
PCIE_TX4N AE25 PEG_D2R_C_N<4> C8464 0.1uF PEG_D2R_N<4>
PCIE_TX5P AE28 PEG_D2R_C_P<5> C8465 0.1uF PEG_D2R_P<5>
PCIE_TX5N AD28 PEG_D2R_C_N<5> C8466 0.1uF PEG_D2R_N<5>
PCIE_TX6P AD27 PEG_D2R_C_P<6> C8467 0.1uF PEG_D2R_P<6>
PCIE_TX6N AC27 PEG_D2R_C_N<6> C8468 0.1uF PEG_D2R_N<6>
PCIE_TX7P AC25 PEG_D2R_C_P<7> C8469 0.1uF PEG_D2R_P<7>
PCIE_TX7N AB25 PEG_D2R_C_N<7> C8470 0.1uF PEG_D2R_N<7>
PCIE_TX8P AB28 PEG_D2R_C_P<8> C8471 0.1uF PEG_D2R_P<8>
PCIE_TX8N AA28 PEG_D2R_C_N<8> C8472 0.1uF PEG_D2R_N<8>
PCIE_TX9P AA27 PEG_D2R_C_P<9> C8473 0.1uF PEG_D2R_P<9>
PCIE_TX9N Y27 PEG_D2R_C_N<9> C8474 0.1uF PEG_D2R_N<9>
PCIE_TX10P Y25 PEG_D2R_C_P<10> C8475 0.1uF PEG_D2R_P<10>
PCIE_TX10N W25 PEG_D2R_C_N<10> C8476 0.1uF PEG_D2R_N<10>
PCIE_TX11P W28 PEG_D2R_C_P<11> C8477 0.1uF PEG_D2R_P<11>
PCIE_TX11N V28 PEG_D2R_C_N<11> C8478 0.1uF PEG_D2R_N<11>
PCIE_TX12P V27 PEG_D2R_C_P<12> C8479 0.1uF PEG_D2R_P<12>
PCIE_TX12N U27 PEG_D2R_C_N<12> C8480 0.1uF PEG_D2R_N<12>
PCIE_TX13P U25 PEG_D2R_C_P<13> C8481 0.1uF PEG_D2R_P<13>
PCIE_TX13N T25 PEG_D2R_C_N<13> C8482 0.1uF PEG_D2R_N<13>
PCIE_TX14P T28 PEG_D2R_C_P<14> C8483 0.1uF PEG_D2R_P<14>
PCIE_TX14N R28 PEG_D2R_C_N<14> C8484 0.1uF PEG_D2R_N<14>
PCIE_TX15P R27 PEG_D2R_C_P<15> C8485 0.1uF PEG_D2R_P<15>
PCIE_TX15N P27 PEG_D2R_C_N<15> C8486 0.1uF PEG_D2R_N<15>
PCIE_CALRP AD24 GPU_PCIE_CALRP
PCIE_CALRN AE24 GPU_PCIE_CALRN
PCIE_CALI AB24 GPU_PCIE_CALI
PP1V2_D3C
R8495 2.0K 1% 1/16W MF-LF 402
R8497 1.47K 1% 1/16W MF-LF 402
R8496 562 1% 1/16W MF-LF 402

ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	70	87

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GPU VCore Supply

PP5V_S5
PPBUS_G3H

C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM1 603
C8502 2.2UF 20% 6.3V CERM1 603

U8500 ISL62698CRZ QFN
CRITICAL
PVCC VCC
VIN FSET EN FCCM PGOOD COMP FB VO
UG BOOT PHASE ISEN LG PGND
THRML PAD

R8504 0 5% 1/16W MF-LF 402
GPUVCORE_EN
GPUVCORE_FSET
GPUVCORE_FCCM
P1V2R2V5D3C_EN_LS5V
GPUVCORE_COMP
GPUVCORE_FB

R8508 150K 1% 1/16W MF-LF 402
GPUVCORE_COMP_R
C8507 15pF 5% 50V CERM 402
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
NO STUFF R8505 0 5% 1/16W MF-LF 402
C8508 470pF 10% 50V CERM 402
GND_GPUVCORE_SGND

XW8500 SM
XW8501 SM
XW8502 SM

GPUVCORE_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R8509 4.7 5% 1/16W MF-LF 402
C8509 0.22UF 20% 6.3V XSR 402
Stuff 4.7ohm for decreased Slew rate

GPUVCORE_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
GPUVCORE_BOOT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
GPUVCORE_PHASE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
GPUVCORE_ISEN
GPUVCORE_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

R8510 5.11K 1% 1/16W MF-LF 402

CRITICAL Q8520 RJK0305DPB LFPAK
CRITICAL Q8521 RJK0301DPB LFPAK
CRITICAL Q8522 RJK0301DPB LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402

CRITICAL C8530 33uF 20% 16V POLY CASED2E-SM

GND_GPUVCORE_PGND

GPU VCore Current Sense

PP3V3_S0

CRITICAL R8597 10KOHM-5% 0603-LF
NO STUFF R8594 1K 1% 1/16W MF-LF 402
R8596 1K 1% 1/16W MF-LF 402

Placement Note:
Keep C8590, C8591
R8590, R8594 and R8597
close to inductor

C8590 0.47UF 10% 6.3V CERM-XSR 402
C8591 0.22UF 10% 6.3V CERM-XSR 402

R8593 20.0K 1% 1/16W MF-LF 402
GPUISENS_NEG
R8591 20.0K 1% 1/16W MF-LF 402
GPUISENS_RC
R8590 649 1% 1/16W MF-LF 402
GPUISENS_POS

CRITICAL L8520 1.2UH FDA1055

C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402

CRITICAL U8595 HPA00141AIDCKR SC70-5
GPUVCORE_IOUT

PPVCORE_D3C_GPU
Vout = 1.10V / 0.95V
18A max output
(L8520 limit)

<Ra> R8521 3.01K 1% 1/16W MF-LF 402
NO STUFF R8520 0 5% 1/16W MF-LF 402
GPUVCORE_FB_RC
<Rb> R8522 5.11K 1% 1/16W MF-LF 402
(GPUVCORE_FB)
NO STUFF C8520 0.0022uF 10% 50V CERM 402

C8540 22UF 20% 6.3V CERM 805
C8541 22UF 20% 6.3V CERM 805
C8542 330UF 20% 2.5V POLY CASE-D2E-LF
C8543 330UF 20% 2.5V POLY CASE-D2E-LF

<Rc> R8523 7.32K 1% 1/16W MF-LF 402
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

PP3V3_D3C
R8526 10K 5% 1/16W MF-LF 402
GPU_VCORE_HIGH
R8525 10K 5% 1/16W MF-LF 402
GPU_VCORE_HIGH_RC
Q8523 2N7002DW-X-F SOT-363
C8523 0.022uF 10% 16V CERM-XSR 402
GPU_VCORE_LOW
Q8523 2N7002DW-X-F SOT-363
R8524 10K 5% 1/16W MF-LF 402

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

Q8575 SI3446DV TSOP-LF
PPVCORE_D3C_GPU
GPUBB_EN_L

CRITICAL U8550 FAN2558 SOT23-6-LF
VIN VOUT PG EN GND ADJ

PP3V3_D3C
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM1 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22UF 20% 6.3V CERM 805
PPBB_S0_GPU
Vout = (1.58V /) 1.50V
180mA max output
(LDO limit)

GPUBBP_ADJ
NO STUFF R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
<Rc>
C8557 22UF 20% 6.3V CERM 805

GPUBBP_ADJ_LOW
NO STUFF Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

PPVCORE_D3C_GPU
For proper M56 power sequence, this pull-up must be powered before VCore

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

R8570 4.7K 1% 1/16W MF-LF 402
GPUBB_EN_L
NO STUFF C8570 0.0022uF 10% 50V CERM 402
GPU_BB_CTL
R8561 0 5% 1/16W MF-LF 402
GPU_GENERICD
GPUBB_EN
Q8570 2N7002 SOT23-LF
R8560 10K 5% 1/16W MF-LF 402

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.

PP3V3_D3C
C8580 10UF 20% 6.3V X5R 603
GPUBB_EN

U8580 MAX1673 SOI
CRITICAL
SHDN_L IN FB CAP+ CAP- OUT LIN/SKIP_L GND

GPUBBN_CAPP
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
C8581 2.2uF 20% 6.3V CERM1 603
GPUBBN_CAPN
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

GPUBBN_FB
<Ra> R8587 68.1K 1% 1/16W MF-LF 402
<Rb> R8588 11.3K 1% 1/16W MF-LF 402
C8589 22UF 20% 6.3V CERM 805
PNBB_S0_GPU

Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA
Vout = -0.55V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164 REV. 06004
	SCALE NONE	SHT 71 OF 87

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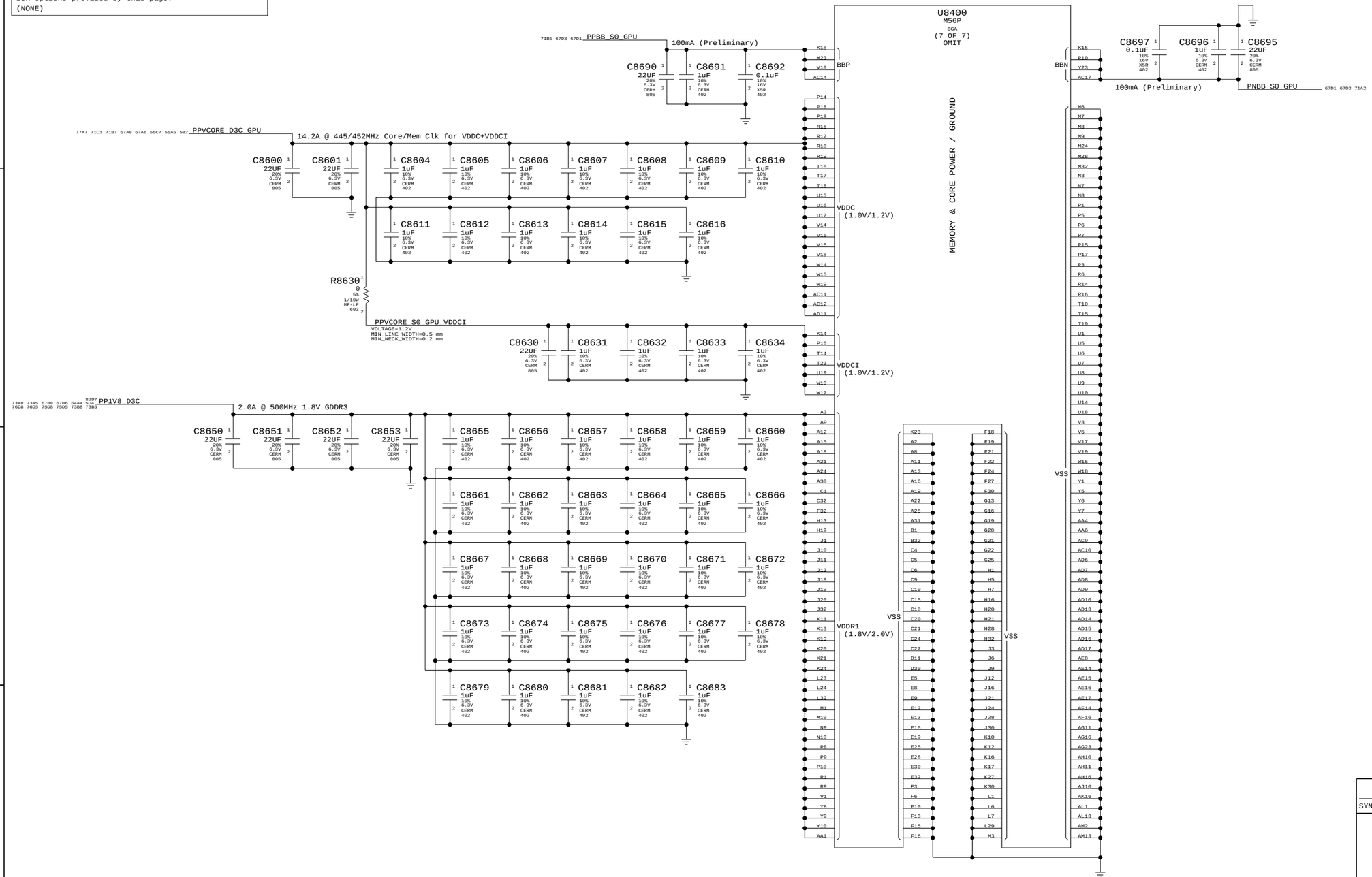
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7164	06004

SCALE	SHT	OF
NONE	72	87

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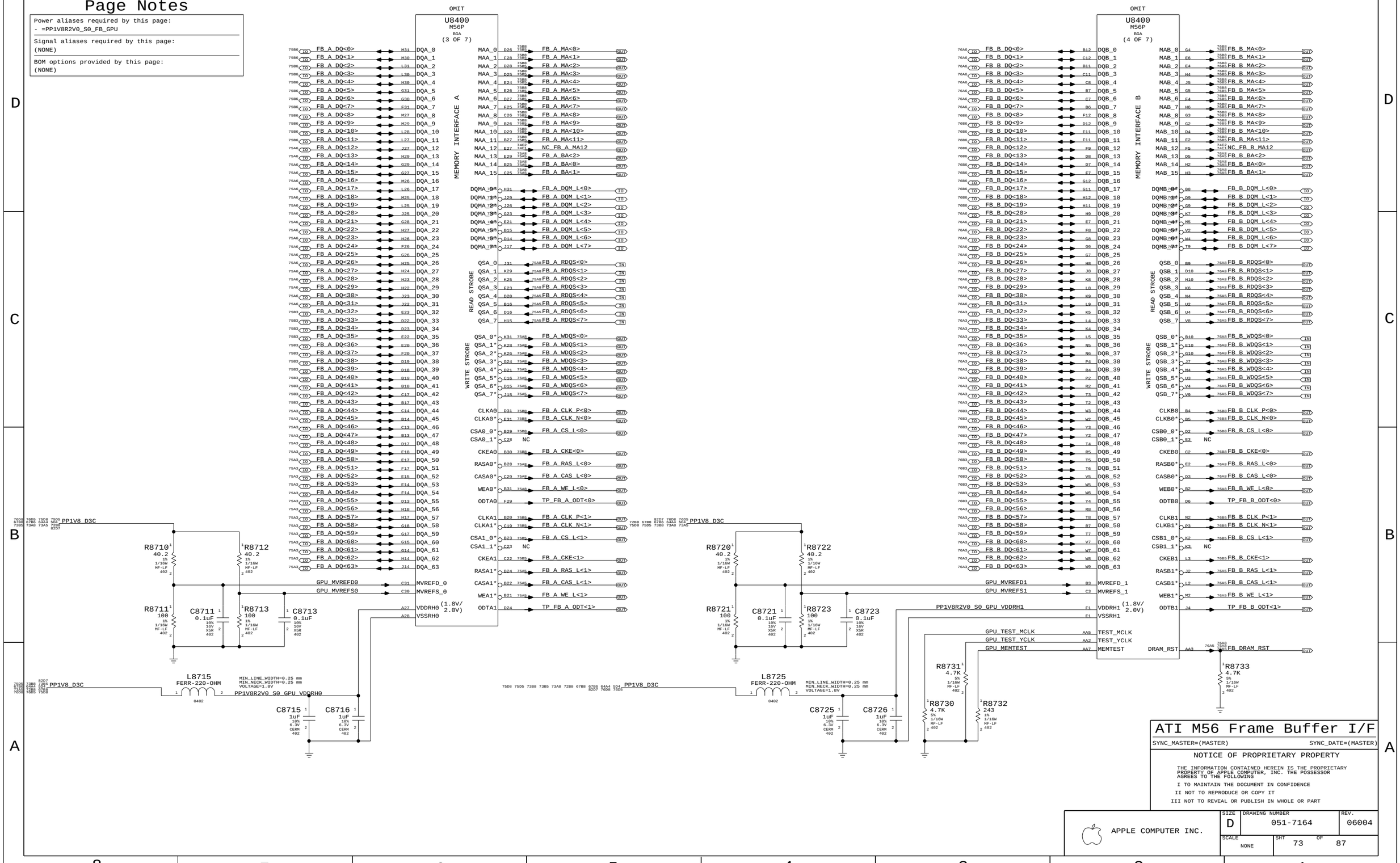
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

77D2 77C6 77B7 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8800 10K 5% 1/16W MF-LF 402
NO STUFF R8802 10K 5% 1/16W MF-LF 402
NO STUFF R8804 10K 5% 1/16W MF-LF 402
NO STUFF R8806 10K 5% 1/16W MF-LF 402
NO STUFF R8809 10K 5% 1/16W MF-LF 402
GPU_MEM_256M R8812 10K 5% 1/16W MF-LF 402
GPU_MEM_256M R8824 10K 5% 1/16W MF-LF 402

GPU_DEEPMH_EN R8801 10K 5% 1/16W MF-LF 402
NO STUFF R8803 10K 5% 1/16W MF-LF 402
R8805 10K 5% 1/16W MF-LF 402
NO STUFF R8808 10K 5% 1/16W MF-LF 402
GPU_MEM_64M R8813 10K 5% 1/16W MF-LF 402
NO STUFF R8811 10K 5% 1/16W MF-LF 402
GPU_MEM_NOT_SAM R8827 10K 5% 1/16W MF-LF 402

		Serial ROM	TestBus	Misc	Straps
77D3	GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
77D3	GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
77D3	GPU_GPIO_2		TESTIN[2]		Reserved
77D3	GPU_GPIO_3		TESTIN[3]		Reserved
77D3	GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
77D3	GPU_GPIO_5		TESTIN[5]		Reserved
77D3	GPU_GPIO_6		TESTIN[6]		Reserved
82A4 77D3 74C5	GPU_BLON	ENA_BL	TESTIN[7]		
77D3	GPU_GPIO_8	ROMSO	TESTWR		Reserved
77C3	GPU_GPIO_9	IPD	ROMSI		ROMIDCFG[3]
77C3 74C5	TP_GPU_GPIO_10		ROMSCK	TESTOUT[8]	
77C3	GPU_GPIO_11	IPD		TESTOUT[9]	ROMIDCFG[0]
77C3	GPU_GPIO_12	IPD		TESTOUT[10]	ROMIDCFG[1]
77C3	GPU_GPIO_13	IPD		TESTOUT[11]	ROMIDCFG[2]
77C3 74C5	NC_GPU_GPIO_14			TESTIN[8]	
77C3 74C5 71B4	GPU_VCORE_LOW			TESTIN[9] PWRCNTL	
77C3 74C5 34B4 34B2	GPU_CLK27MSS_IN			SS_IN	
77C3 74C5	NC_GPU_GPIO_17			Thm Mon Int	

GPU_BLON — MAKE_BASE=TRUE — 74C8 77D3 82A4
TP_GPU_GPIO_10 — MAKE_BASE=TRUE — 74C8 77C3
NC_GPU_GPIO_14 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3
GPU_VCORE_LOW — MAKE_BASE=TRUE — 71B4 74C8 77C3
GPU_CLK27MSS_IN — MAKE_BASE=TRUE — 34B2 34B4 74C8 77C3
NC_GPU_GPIO_17 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3

Required for debug access
Required for debug access
Required for debug access
Required for debug access

77D5 74B7 NC_GPU_GPIO_18 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_18 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_19 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_19 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_20 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_20 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_21 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_21 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_22 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_22 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_23 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_23 — 74B8 77D5
77D5 74B6 GPU_MEM_256M — 77D5 74B8 GPU_MEM_256M MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_25 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_25 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_26 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_26 — 74B8 77D5
77D5 74B6 GPU_MEMID — 77D5 74B8 GPU_MEMID MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_28 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_28 — 74B8 77D5
77C5 74B7 NC_GPU_GPIO_29 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_29 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_30 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_30 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_31 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_31 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_32 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_32 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_33 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_33 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_34 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_34 — 74B8 77C5

Renamed signals

77A5 74C1 34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_CLK27M — 34B2 34B4 74C2 77A5

Unused signals

77A5 74C1 NC_GPU_XTALOUT — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_XTALOUT — 74C2 77A5
77A3 74C1 NC_ATI_ROMCS_L — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_ATI_ROMCS_L — 74C2 77A3
74C1 73D5 NC_FB_A_MA12 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_FB_A_MA12 — 73D5 74C2
74C1 73D1 NC_FB_B_MA12 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_FB_B_MA12 — 73D1 74C2
77C3 74C1 NC_GPU_GENERICA — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICA — 74C2 77C3
77C3 74C1 NC_GPU_GENERICB — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICB — 74C2 77C3
77C3 74C1 NC_GPU_GENERICC — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICC — 74C2 77C3
78C3 74C1 NC_GPU_VGA_R — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_R — 74C2 78C3
78C3 74C1 NC_GPU_VGA_G — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_G — 74C2 78C3
78C3 74C1 NC_GPU_VGA_B — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_B — 74C2 78C3
78B3 74C1 TP_GPU_VGA_HSYNC — MAKE_BASE=TRUE — TP_GPU_VGA_HSYNC — 74C2 78B3
78B3 74C1 TP_GPU_VGA_VSYNC — MAKE_BASE=TRUE — TP_GPU_VGA_VSYNC — 74C2 78B3
78B3 74C1 NC_GPU_TV_Y — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_Y — 74C2 78B3
78B3 74B1 NC_GPU_TV_C — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_C — 74B2 78B3
78B3 74B1 NC_GPU_TV_COMP — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_COMP — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAP<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_U_DATAP<3> — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAN<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_U_DATAN<3> — 74B2 78B3
78A3 74B1 NC_LVDS_L_DATAP<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_L_DATAP<3> — 74B2 78A3
78A3 74B1 NC_LVDS_L_DATAN<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_L_DATAN<3> — 74B2 78A3
77C3 74B1 NC_ATI_DVPCLK — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_ATI_DVPCLK — 74B2 77C3
77C3 77B3 NC_ATI_DVPCNTL<2..0> — MAKE_BASE=TRUE — NO_TEST=TRUE — ATI_DVPCNTL<2..0>
77B3 NC_ATI_DVPDATA<15..0> — MAKE_BASE=TRUE — NO_TEST=TRUE — ATI_DVPDATA<15..0>

Required for debug access

77B3 77A3 TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

77D2 77C6 77B7 74D6 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402

78A3 GPU_DDC_B_CLK
78A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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D	051-7164	06004
SCALE NONE	SHT 74 OF 87	

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: U8900 DQ0-7 MUST connect to GPU
DQA0-7 or DQA8-15. Bits can be swapped
within byte-lane, but software must know
how these bits are mapped for GPU to support
GDDR3 vendor/device identification scheme.

Connect to designated pin, then GND

Connect to designated pin, then GND

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7164	06004

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CRITICAL
OMIT

U9000
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U9050
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

Connect to designated pin, then GND

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7164	06004

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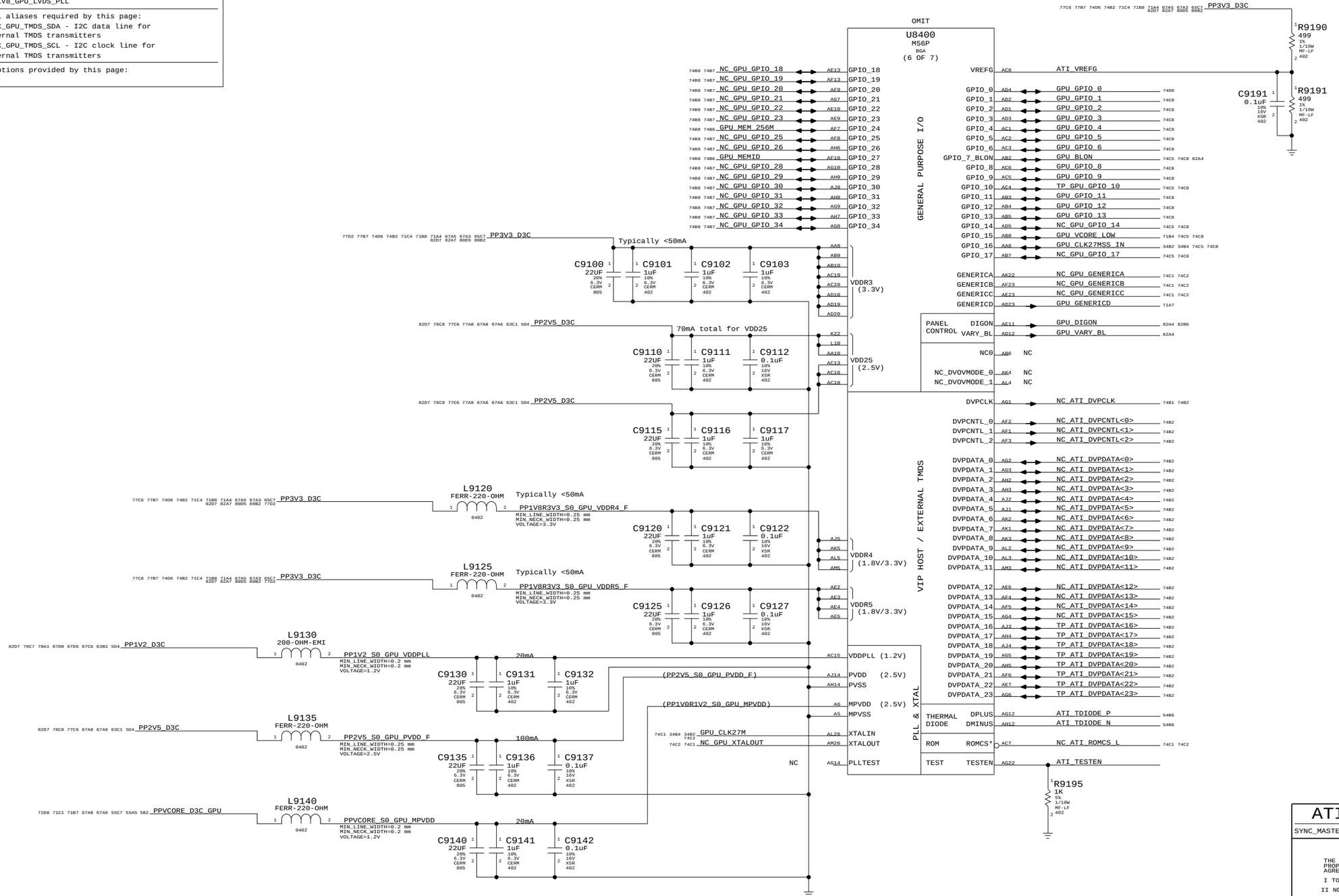
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

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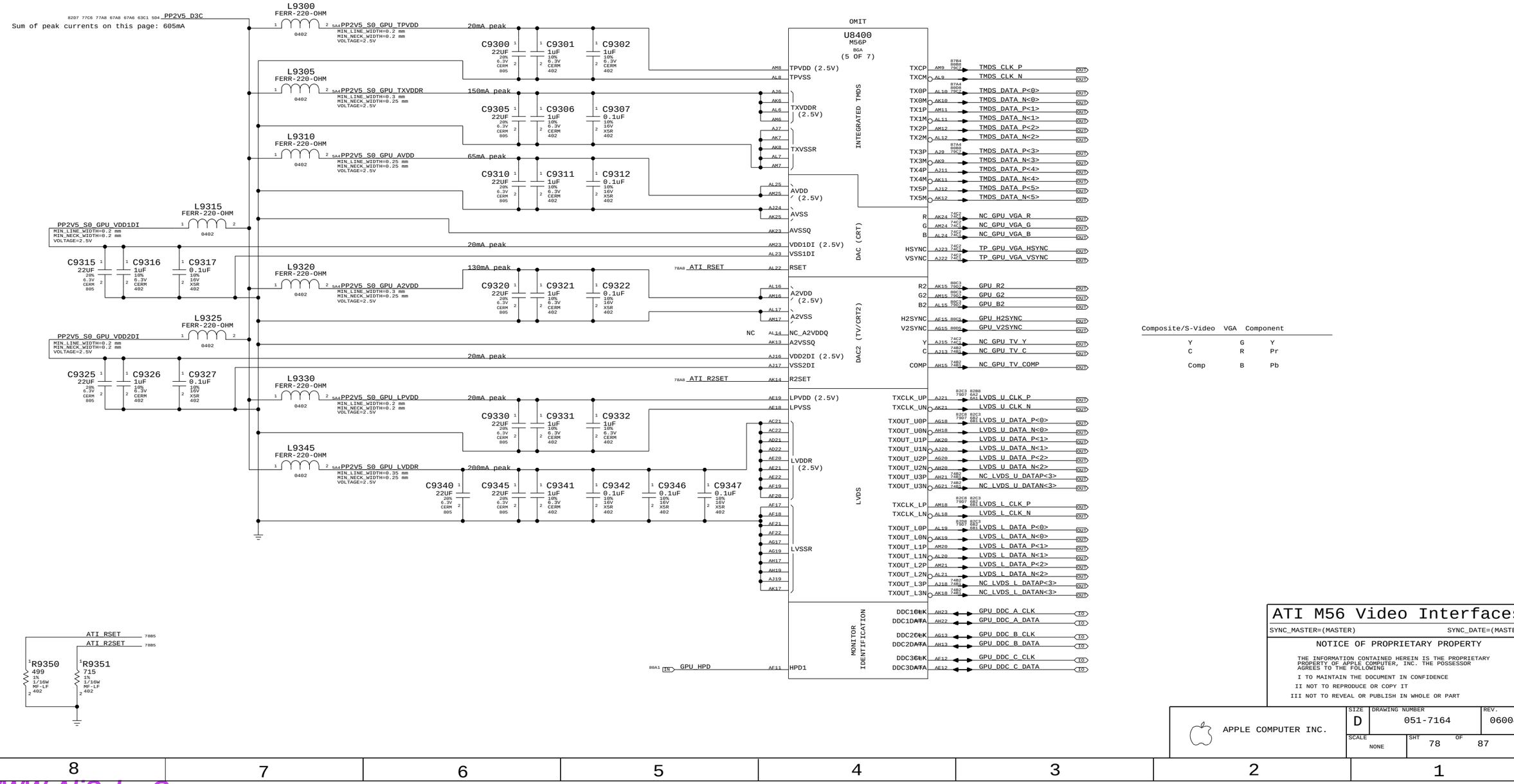
Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Video Interfaces

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LCD (LVDS) INTERFACE

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	LVDS	LVDS	LVDS_U_CLK_CONN_P
	LVDS	LVDS	LVDS_U_CLK_CONN_N
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_CONN_P
	LVDS	LVDS	LVDS_L_CLK_CONN_N
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

PP3V3_S5

C9400 0.0022uF 10% 50V CERM 402

R9400 100K 5% 1/10W MF-LF 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

Q9400 SI3443DV TSOP-LF

PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

LVDS_PANEL_EN

R9494 100K 5% 1/16W MF-LF 402

PP3V3_S0

100K pull-ups are for no-panel case (development). Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

LVDS_CONN_DDC_CLK

LVDS_CONN_DDC_DATA

C9410 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

GND_CHASSIS_LVDS

C9420 0.001uF 20% 50V CERM 402

CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM

PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

LVDS_L_DATA_CONN_N<0>
LVDS_L_DATA_CONN_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_CONN_N
LVDS_L_CLK_CONN_P
LVDS_U_DATA_CONN_N<0>
LVDS_U_DATA_CONN_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_CONN_N
LVDS_U_CLK_CONN_P

C9421 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

518S0289

INVERTER INTERFACE

CRITICAL
L9450 FERR-220-OHM-2A 0603

PPBUS_G3H

PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

PP5V_S0

Q9450 FDG6332C_NL SC70-6 P-CHN

R9450 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V X5R 603

FP_PWR_EN_L

Q9450 FDG6332C_NL SC70-6 N-CHN

INVERTER_BKLTON

R9489 100K 5% 1/16W MF-LF 402

CRITICAL
J9450 SM04B-ACH M-RT-SM

NC
NC

PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

518S0369

L9454 400-OHM-EMI SM-1

INVERTER_PWM

GND_CHASSIS_INVERTER

C9454 0.001uF 20% 50V CERM 402

CRITICAL
L9455 FERR-220-OHM-2A 0603

GND_CHASSIS_INVERTER

PP3V3_S0

PLT_RST_L

INVERTER_PWM_UNBUF

U9453 MC74VHC1G08 SC70

INVERTER_PWM_F

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

C9453 0.1uF 20% 10V CERM 402

Internal Display Connectors

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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TMDS Filtering

Place termination components close to GPU, common mode chokes near connector.

TMDS_DATA_N<0> — TMDS_DATA_RL<0> (VOLTAGE=0V, NO_TEST=TRUE) — R9762 182 1% 1/16W MF-LF 402 — L9743 47nH 0402 — TMDS_DATA_P<0>
CRITICAL L9700 90-OHM-100MA 1210-4SM1 (SYM_VER=1): TMDS_DATA_F_N<0> → TMDS_DATA_F_P<0>

TMDS_DATA_N<1> — TMDS_DATA_RL<1> (VOLTAGE=0V, NO_TEST=TRUE) — R9766 182 1% 1/16W MF-LF 402 — L9744 47nH 0402 — TMDS_DATA_P<1>
CRITICAL L9701 90-OHM-100MA 1210-4SM1 (SYM_VER=1): TMDS_DATA_F_N<1> → TMDS_DATA_F_P<1>

TMDS_DATA_N<2> — TMDS_DATA_RL<2> (VOLTAGE=0V, NO_TEST=TRUE) — R9770 182 1% 1/16W MF-LF 402 — L9745 47nH 0402 — TMDS_DATA_P<2>
CRITICAL L9702 90-OHM-100MA 1210-4SM1 (SYM_VER=1): TMDS_DATA_F_N<2> → TMDS_DATA_F_P<2>

TMDS_CLK_N — R9772 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_N
TMDS_CLK_P — R9774 182 1% 1/16W MF-LF 402 — R9773 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_P
CRITICAL L9706 370-OHM SM (SYM_VER=1): TMDS_CLK_F_N → TMDS_CLK_F_P

TMDS_DATA_N<3> — TMDS_DATA_RL<3> (VOLTAGE=0V, NO_TEST=TRUE) — R9778 182 1% 1/16W MF-LF 402 — L9746 47nH 0402 — TMDS_DATA_P<3>
CRITICAL L9703 90-OHM-100MA 1210-4SM1 (SYM_VER=1): TMDS_DATA_F_N<3> → TMDS_DATA_F_P<3>

TMDS_DATA_N<4> — TMDS_DATA_RL<4> (VOLTAGE=0V, NO_TEST=TRUE) — R9782 182 1% 1/16W MF-LF 402 — L9747 47nH 0402 — TMDS_DATA_P<4>
CRITICAL L9704 90-OHM-100MA 1210-4SM1 (SYM_VER=1): TMDS_DATA_F_N<4> → TMDS_DATA_F_P<4>

TMDS_DATA_N<5> — TMDS_DATA_RL<5> (VOLTAGE=0V, NO_TEST=TRUE) — R9786 182 1% 1/16W MF-LF 402 — L9748 47nH 0402 — TMDS_DATA_P<5>
CRITICAL L9705 90-OHM-100MA 1210-4SM1 (SYM_VER=1): TMDS_DATA_F_N<5> → TMDS_DATA_F_P<5>

VGA SYNC BUFFERS

PP3V3_D3C → U9750 (MC74VHC1G08 5C70) ← GPU_V2SYNC
U9750 → VGA_VSYNC_R — R9750 33 5% 1/16W MF-LF 402 — VGA_VSYNC
C9750 0.1uF 20% 10V CERM 402

PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

PP3V3_D3C → U9751 (MC74VHC1G08 5C70) ← GPU_H2SYNC
U9751 → VGA_HSYNC_R — R9751 33 5% 1/16W MF-LF 402 — VGA_HSYNC
C9751 0.1uF 20% 10V CERM 402

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_B2 (DAC2 Comp) — R9740 75 1% 1/16W MF-LF 402 — CRITICAL FL9740 LCFILTER SM-220MHZ-LF — VGA_B
C9740 3.3pF 0.25% 50V CERM 402

GPU_G2 (DAC2 Y) — R9741 75 1% 1/16W MF-LF 402 — CRITICAL FL9741 LCFILTER SM-220MHZ-LF — VGA_G
C9741 3.3pF 0.25% 50V CERM 402

GPU_R2 (DAC2 C) — R9742 75 1% 1/16W MF-LF 402 — CRITICAL FL9742 LCFILTER SM-220MHZ-LF — VGA_R
C9742 3.3pF 0.25% 50V CERM 402

DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0 → PP5V_S0_DDC_F (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)
L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC_F → PP5V_S0_DDC (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL J9700 QH11121-RIG02-4F F-RT-TH-DVI

J9700		J9700	
GND_CHASSIS_DVI_BOT	33	31	
TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
		9	TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0>	18	2	TMDS_DATA_F_P<2>
		10	TMDS_DATA_F_P<1>
	19	3	
TMDS_DATA_F_N<5>	20	11	
		4	TMDS_DATA_F_N<4>
TMDS_DATA_F_P<5>	21	12	TMDS_DATA_F_N<3>
		5	TMDS_DATA_F_P<4>
	22	13	TMDS_DATA_F_P<3>
		6	DVI_DDC_CLK_R
		14	(PP5V_S0_DDC)
TMDS_CLK_F_P	23	7	DVI_DDC_DATA_R
		15	
TMDS_CLK_F_N	24	8	VGA_VSYNC
		16	DVI_HPD_R
VGA_B	C3	C1	VGA_R
	C5B	C5A	
VGA_HSYNC	C4	C2	VGA_G
	34	32	
GND_CHASSIS_DVI_TOP			

514-0278

PLACE NEAR C5A & C5B
R9730 0 5% 1/16W MF-LF 402
C9710 0.01uF 20% 50V CERM 603
C9714 100pF 5% 50V CERM 402
R9731 0 5% 1/16W MF-LF 402 — GND_CHASSIS_DVI_TOP
PLACE NEAR 3, 11 & 19

Isolation required for DVI power switch

D9710 SOD-123 B0530WXF
PP5V_S0_DDC_PULLUPS (VOLTAGE=5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)
R9710 4.7K 5% 1/16W MF-LF 402 — PP5V_S0_DDC_PULLUPS
R9712 4.7K 5% 1/16W MF-LF 402 — PP3V3_D3C
C9711 100pF 5% 50V CERM 402 — GND
C9713 100pF 5% 50V CERM 402 — GND
C9714 100pF 5% 50V CERM 402 — GND_CHASSIS_DVI_BOT

3V LEVEL SHIFTERS

R9711 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK
R9713 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA
R9714 100 5% 1/16W MF-LF 402 — DVI_HPD
Q9711 2N7002DW-X-F SOT-363 — GPU_DDC_A_CLK
Q9711 2N7002DW-X-F SOT-363 — GPU_DDC_A_DATA
Q9714 2N7002DW-X-F SOT-363 — GPU_HPD
Q9715 2N7002DW-X-F SOT-363 — SB_DVI_HPD
R9720 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_CLK
R9721 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_DATA
R9722 270K 5% 1/16W MF-LF 402 — GPU_HPD
R9723 270K 5% 1/16W MF-LF 402 — SB_DVI_HPD
GPU_HPD_BILAT — PP5V_S0
GPU_SIGNAL_ENABLE
R9715 20K 5% 1/16W MF-LF 402 — GND
MAKE_BASE=TRUE

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P
	TMDS	TMDS	TMDS_CLK_R_N
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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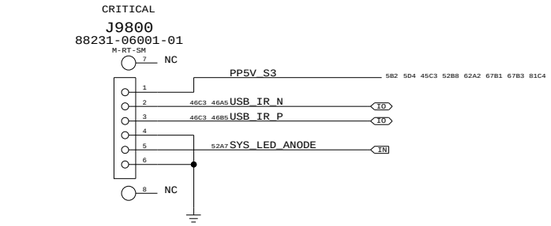
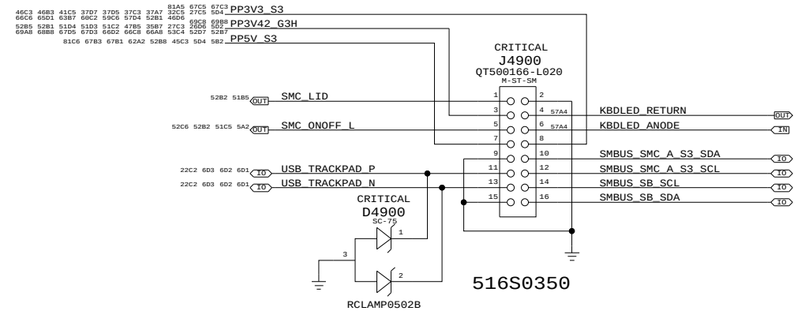
IR & Sleep LED Connector



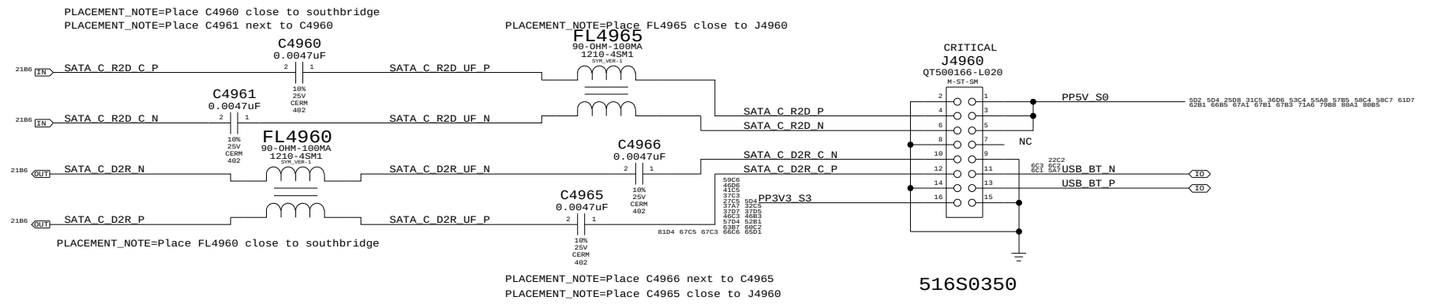
518S0474

Top-Case Connector



516S0350

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M57 SPECIFIC CONNECTORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	81	87

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LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_L_CLK_P
=LVDS_PD_L_CLK_N
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
=LVDS_PD_U_CLK_P
=LVDS_PD_U_CLK_N

LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF

PGOOD Monitor for GPU Rails

D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.
D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.

PP3V3_D3C
PP2V5_D3C
PP1V8_D3C
PP1V2_D3C
PP3V3_S0

R9994 124K 1% 1/16W MF-LF 402
R9992 237K 1% 1/16W MF-LF 402
R9990 365K 1% 1/16W MF-LF 402
C9990 0.1UF 20% 10V CERM 402
R9997 10K 5% 1/16W MF-LF 402
C9991 0.1UF 20% 10V CERM 402

U9990 LTC2903 TSOT-23
V1 CRITICAL
V2 D3CPGOOD_2V5_DIV
V3 D3CPGOOD_1V8_DIV
V4 D3CPGOOD_1V2_DIV
RST* S0PGOOD_PWROK
GND
D3CPGOOD_PWROK

U9991 MC74VHC1G08 SC70
S0PGOOD_PWROK
S0D3CPGOOD_PWROK

R9995 100K 1% 1/16W MF-LF 402
C9995 0.1UF 20% 10V CERM 402
R9993 100K 1% 1/16W MF-LF 402
C9993 0.1UF 20% 10V CERM 402
R9991 100K 1% 1/16W MF-LF 402
C9992 0.1UF 20% 10V CERM 402
R9996 470K 5% 1/16W MF-LF 402
C9996 1UF 10% 6.3V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

PP3V3_S0
PP2V5_S0
C9985 0.1UF 20% 10V CERM 402
C9980 0.1UF 20% 10V CERM 402
GPU_DIGON
LVDS_MUX_SEL_GPU
U9985 MC74VHC1G08 SC70
GPU_DIGON_AND_SELECTED
CRITICAL
U9980 SN74LVC1G132 SC70-5
PP3V3_LCD_SW
R9980 10K 5% 1/16W MF-LF 402
PANEL_PWR_ON
R9981 13.3K 1% 1/16W MF-LF 402

Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU DDC Pass FETs

GPU_SIGNAL_ENABLE
PP3V3_D3C
R9970 15.8K 1% 1/16W MF-LF 402
Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_CLK
LVDS_CONN_DDC_CLK
MAKE_BASE=TRUE
R9971 15.8K 1% 1/16W MF-LF 402
Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_DATA
LVDS_CONN_DDC_DATA
MAKE_BASE=TRUE

LVDS I/F Mux

PP2V5_S0
C9950 0.1UF 20% 10V CERM 402
VDD
U9950 CRITICAL CBTV4020 BGA-LF SYM_VER-3

NB LVDS I/F

LVDS_B_DATA_N<2> F1 DA0
LVDS_B_DATA_N<0> H1 DA1
LVDS_B_DATA_P<0> K1 DA2
K3 DA3
LVDS_A_CLK_P K4 DA4
LVDS_A_CLK_N K6 DA5
J7 DA6
LVDS_A_DATA_N<0> K9 DA7
LVDS_A_DATA_P<0> J10 DA8
LVDS_A_DATA_P<2> G10 DA9
LVDS_A_DATA_N<2> E10 DA10
LVDS_A_DATA_N<1> C10 DA11
LVDS_A_DATA_P<1> A10 DA12
A8 DA13
LVDS_B_DATA_P<1> A7 DA14
LVDS_B_DATA_N<1> A5 DA15
B4 DA16
LVDS_B_CLK_N A2 DA17
LVDS_B_CLK_P B1 DA18
LVDS_B_DATA_P<2> D1 DA19

GPU LVDS I/F

LVDS_U_DATA_N<2> G1 DB0*
LVDS_U_DATA_N<0> J1 DB1*
LVDS_U_DATA_P<0> K2 DB2*
J4 DB3*
LVDS_L_CLK_P K5 DB4*
LVDS_L_CLK_N K7 DB5*
K8 DB6*
LVDS_L_DATA_N<0> K10 DB7*
LVDS_L_DATA_P<0> H10 DB8*
LVDS_L_DATA_P<2> F10 DB9*
LVDS_L_DATA_N<2> D10 DB10*
LVDS_L_DATA_N<1> B10 DB11*
LVDS_L_DATA_P<1> A9 DB12*
B7 DB13*
LVDS_U_DATA_P<1> A6 DB14*
LVDS_U_DATA_N<1> A4 DB15*
A3 DB16*
LVDS_U_CLK_N A1 DB17*
LVDS_U_CLK_P C1 DB18*
LVDS_U_DATA_P<2> E1 DB19*

GND
H6 H5 G3 G2 D4 D3 C6 C5

DH0 F2 LVDS_U_DATA_CONN_N<2>
DH1 H2 LVDS_U_DATA_CONN_N<0>
DH2 J2 LVDS_U_DATA_CONN_P<0>
DH3 J3 NC
DH4 J5 LVDS_L_CLK_CONN_P
DH5 J6 LVDS_L_CLK_CONN_N
DH6 J8 NC
DH7 J9 LVDS_L_DATA_CONN_N<0>
DH8 H9 LVDS_L_DATA_CONN_P<0>
DH9 F9 LVDS_L_DATA_CONN_P<2>
DH10 E9 LVDS_L_DATA_CONN_N<2>
DH11 C9 LVDS_L_DATA_CONN_N<1>
DH12 B9 LVDS_L_DATA_CONN_P<1>
DH13 B8 NC
DH14 B6 LVDS_U_DATA_CONN_P<1>
DH15 B5 LVDS_U_DATA_CONN_N<1>
DH16 B3 NC
DH17 B2 LVDS_U_CLK_CONN_N
DH18 C2 LVDS_U_CLK_CONN_P
DH19 E2 LVDS_U_DATA_CONN_P<2>

SEL E3 LVDS_MUX_SEL_GPU_L

NOTE: SEL = LOW selects port B

Panel/Backlight Control Mux

PP3V3_S0
C9960 0.1UF 20% 10V CERM 402
CRITICAL
U9960 74CBTLV3257 QFN SYM_VER-2
VCC
GND
THRML PAD

LVDS_VDDEN 1B1
GPU_DIGON 1B2
LVDS_BKLTEN 2B1
GPU_BLON 2B2
LVDS_BKLTCTL 3B1
GPU_VARY_BL 3B2
S0PGOOD_PWROK 4B1
S0D3CPGOOD_PWROK 4B2
LVDS_MUX_SEL_GPU_MUXED S
OE*

1A LVDS_PANEL_EN
2A INVERTER_BKLTON
3A INVERTER_PWM_UNBUF
4A PGOOD_MUXED_S0_OR_S0D3C

PP3V3_S0
C9961 0.1UF 20% 10V CERM 402
PLT_RST_L
LVDS_MUX_SEL_GPU
U9961 MC74VHC1G08 SC70
NO STUFF
R9962 0 5% 1/16W MF-LF 402
R9961 100K 5% 1/16W MF-LF 402
R9960 10K 5% 1/16W MF-LF 402

NOTE: S = HIGH selects xB2

LVDS_MUX_SEL_GPU
LVDS_MUX_SEL_GPU
MAKE_BASE=TRUE
LVDS_MUX_SEL_GPU

NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU

LVDS Interface Pull-downs

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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Revision History

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SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	83	87

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	84	87

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GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3SS_TO_5SS	*	Y	=3S_OHM_SE	=5S_OHM_SE	=3S_5S_OHM_SE	=STANDARD	=STANDARD
FB_4GS	*	Y	=4G_OHM_SE	=4G_OHM_SE	=4G_OHM_SE	=STANDARD	=STANDARD
FB_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5A4 7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5A7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5A4 7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5B7 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5B7 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5A7 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5B7 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5B4 7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	5B4 7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	5C4 7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5B4 14B7 23C3 61C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5C4 61C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 33C4 34D3 34D5
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 33C4 34D3 34D5
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 61B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 61A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61A3

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 48B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 48B3

TMDS	TMDS	TMDS_CLK_P	78C3 79C7 80B8
TMDS	TMDS	TMDS_CLK_N	78C3 79C7 80C8
TMDS	TMDS	TMDS_DATA_P<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_N<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_P<2..0>	78C3 79C7 80C8 80D8
TMDS	TMDS	TMDS_DATA_N<2..0>	78C3 79C7 80C8 80D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	80A5 80C6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	80B3 80B5 80C6 80D1 80D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	80B3 80B5 80C6 80D1 80D6

M57 NET PROPERTIES

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